* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] It is the manufacture approach of a semiconductor device of having provided the process which forms the dielectric thin film which consists of a compound expressed with the following general formula (1) on a semi-conductor layer, and is ABO3. .... (1)
(A is at least one sort of elements chosen from the group which consists of calcium, Ba, Sr, Pb, and La here, and B is at least one sort of elements chosen from the group which consists of Zr and Ti)
Formation of said dielectric thin film is the manufacture approach of the semiconductor device characterized by being carried out at the temperature of 1000 degrees C or less to the bottom of the pressure below 400 Torr by the chemical vapor deposition using the material gas containing beta diketone complex compound of said element A, beta diketone complex compound of said element B, and an oxidizer.
[Claim 2] How to be the manufacture approach of a semiconductor device according to claim 1, and to perform said chemical vapor deposition under reaction rate-limiting conditions.
[Claim 3] It is the approach which is the manufacture approach of a semiconductor device according to claim 2, and is performed at temperature with said chemical vapor deposition lower than which pyrolysis temperature of beta diketone complex of said element A, and beta diketone complex of said element B.
[Claim 4] It is the approach by which it is the manufacture approach of a semiconductor device given in any 1 term 3 of claims 1-3, and said chemical vapor deposition is performed under the conditions from which the amount of supply of beta diketone complex of said element B is a mole ratio, and becomes 5 or more times of the amount of supply of beta diketone complex of said element A.
[Claim 5] The approach it is the manufacture approach of a semiconductor device given in any 1 term of claims 1-4, and the compound expressed with said general formula (1) is Bax Sr1-x TiO3 (0<=x<=1).
[Claim 6] The approach it is the manufacture approach of a semiconductor device given in any 1 term of claims 1-5, and the ligand of the aforementioned beta diketone complex compound is dipivaloyl methane (DPM;C11H19O2).
[Claim 7] The approach are the manufacture approach of the semiconductor device a publication and said oxidizer contains molecular oxygen or N2 O in any 1 term of claims 1-6.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the manufacture approach of a semiconductor device of having provided the capacitor, like DRAM. More specifically, it is related with the approach of forming the capacitor insulator layer (storage capacitance film) of this semiconductor device.
[0002]
[Description of the Prior Art] A capacitor is an important component in a semiconductor integrated circuit. For example, by combining a transistor and a capacitor, it consists of dynamic random access memory (DRAM) which is one sort of a semiconductor memory so that the writing and read-out of data may be performed. Moreover, also in other semiconductor integrated circuits, the capacitor is widely used as a component which accumulates a charge.
[0003] The capacitor in a semiconductor integrated circuit consists of a lower electrode which consists of a conductor on a semi-conductor substrate or this substrate, a capacitor insulator layer by which the laminating was carried out on this lower electrode, and an up electrode by which the laminating was carried out on this insulator layer. As this capacitor insulator layer, silicon oxide (SiO2) or silicon nitride (Si3 N4) is used with the conventional capacitor for integrated circuits.
[0004] By the way, it is required that the capacitor in which high integration of a semiconductor device and large capacity-ization of storage capacity followed on progressing quickly, and had big storage capacitance should be formed in a narrow plane region. Making thickness of a capacitor insulator layer thin and increasing the capacitor capacity per effective unit area as the first means which fills this demand, is performed. Moreover, as the second means, increasing the effective-surface product of a capacitor is performed by adopting three-dimensional structure. As an example of this second means, the trench capacitor technique and the SUTAKKUTO capacitor technique are known. A trench capacitor technique increases the effective area of a capacitor by forming a trench slot in a lower electrode (for example, silicon substrate), and forming a capacitor along the front face of this trench slot. Moreover, with the SUTAKKUTO capacitor technique, a big capacitor area is secured by carrying out the laminating of the one or more capacitors, and forming them on a transistor, without sacrificing a degree of integration.
[0005] However, since leakage current increases as the storage capacitance film is made thin, it is also becoming difficult technically for there to be a limit in the thin film-ization and to complicate a spacial configuration further. For this reason, as long as silicon oxide (SiO2) or silicon nitride (Si3 N4) was used as a capacitor insulator layer, it was difficult to realize DRAM with a still higher degree of integration. In fact, high integration DRAM more than a gigabit is not yet realized.
[0006] In order to attain the much more detailed-izing and high integration from such a situation, it is becoming indispensable to use the high dielectric constant ingredient with a dielectric constant higher than the conventional insulator layer as a capacitor insulator layer. Then, recent years and SiO2 Si3 N4 Using the high dielectric materials which have the crystal structure of perovskite molds, such as strontium titanate (SrTiO3) with a high dielectric constant, barium titanate strontium (Bax Sr1-x TiO3),

and PZT (PbZrx Ti1-x O3), is examined. These high dielectric materials are 20 time -1,000 from silicon oxide. It has the high dielectric constant more than twice.
[0007] However, when these high dielectric materials are used for a capacitor insulator layer, there is another problem which is described below.
[0008] Generally, since these high dielectric films have small forbidden-band width of face, leakage current tends to flow at the time of electrical-potential-difference impression. For this reason, when it thin-film-izes in order to secure a required capacitor capacity in case it is used for the capacitor of DRAM, there is a problem that leakage current becomes excessive. Moreover, since the high dielectric film which has the perovskite crystal structure has the property in which a dielectric constant falls when it is thin-film-ized, even if it thin-film-izes with much trouble, comparatively [the], the problem that capacitor capacity does not increase is. Therefore, even when using the above-mentioned high dielectric materials for a capacitor insulator layer, capacitor capacity sufficient by just it cannot be obtained, but it is necessary to use together the same spacial configuration as a trench capacitor technique and a SUTAKKUTO capacitor technique too.
[0009] When using a spacial configuration together, a high dielectric thin film must be formed by good step coverage on the front face which has irregularity. However, sputtering conventionally used for formation of the above-mentioned quantity dielectric thin film is inferior to step coverage. Therefore, in order to use a spacial configuration together, to form the above-mentioned quantity dielectric thin film not by sputtering but by the chemical vapor deposition (CVD method) excellent in step coverage is needed. However, the CVD method which can form the thin film of uniform thickness which consists of the above-mentioned high dielectric materials which are multiple oxides by good step coverage on a substrate with a level difference is not known. For this reason, it is difficult, consequently it is SiO2 to use these high dielectric thin films for a capacitor insulator layer, and to use a spacial configuration together. Si3 N4 As high in a degree of integration a semiconductor device as the semiconductor device using the storage capacitance film is not yet obtained. It will be as follows if this problem is explained more to a detail.
[0010] MOCVD which generally uses an organic metal as a raw material in case a metal oxide film is formed with a CVD method (metal organic CVD) Law is adopted. although the high dielectric materials which have the above-mentioned perovskite crystal structure are also metallic oxides, since it consists of two or more kinds of metallic oxides -- the thin film -- MOCVD -- in forming by law, there are the following problems. That is, it is indispensable for it not to be confused and to form the crystal structure of a perovskite mold, in order to obtain a thin film with a desired high dielectric constant, and in order to attain this, it is necessary to press down the gap from the stoichiometry of a crystal presentation to **10% or less. the case where precise presentation control of such multiple oxide film needs to be attained -- MOCVD -- the rate of sedimentation of a thin film -- supply -- it is carried out under the conditions which become rate-limiting. supply -- since the pyrolysis reaction of a raw material is quick under rate-limiting conditions, the alimentation proportional to the amount of supply of a raw material is obtained. Therefore, in CVD such under supply rate-limiting, the presentation of the multiple oxide to deposit is controllable to a precision by controlling the amount of supply of each raw material to a precision. Control of the amount of supply about each raw material is controllable by controlling CVD conditions, such as raw material temperature, a raw material container pressure, and a raw material bubbling quantity of gas flow, to a precision. such an approach -- Bax Sr1-x TiO3 etc. -- it is used for formation of high-temperature superconductor film, such as a dielectric thin film and YBa2 Cu3 O7-d.
[0011] however, the above supplies -- although precise presentation control becomes possible in CVD in the rate-limiting bottom, it is inferior to step coverage for the following reason. That is, under such supply rate-limiting conditions, shortly after a raw material reaches a substrate, a decomposition reaction will be caused and deposited on a substrate front face, without fully spreading. Therefore, uniform thickness cannot be obtained when the part which a raw material tends to reach like trench structure, and the part which cannot reach easily exist. Therefore, MOCVD under supply rate-limiting does not suit the purpose of using together a spacial configuration like a trench capacitor and a SUTAKKUTO capacitor, and cannot become a technique for corresponding to a gigabit generation.

[0012]
[Problem(s) to be Solved by the Invention] This invention is made in view of the above-mentioned situation. The technical problem SiO2 used conventionally and Si3 N4 etc. -- the thin film of a high dielectric compound with a high dielectric constant -- Namely, in case the semiconductor device which makes thin films, such as SrTiO3, Bax Sr1-x TiO3, and PZT, a capacitor insulator layer is manufactured It is offering the approach of forming these quantities dielectric thin film by uniform thickness on a substrate, and forming by good step coverage also on the substrate which has a level difference especially. It becomes possible to become possible at the same time it uses a high dielectric thin film as a capacitor insulator layer to use together a spacial configuration like a trench capacitor and a SUTAKKUTO capacitor, as a result to manufacture a semiconductor device with a more high degree of integration by such approach.
[0013]
[Means for Solving the Problem] Even if artificers are high dielectric thin films, such as SrTiO3, Bax Sr1-x TiO3, and PZT, wholeheartedly as a result of research, while they choose a specific raw material As it fully spread, when performing CVD on the substrate front face on attainment and this front face, without a raw material decomposing in a gaseous phase, it came to complete a header and this invention for the ability of the thin film which has uniform thickness to be formed also on a substrate front face with a level difference.
[0014] Namely, the manufacture approach of the semiconductor device by this invention is the manufacture approach of a semiconductor device of having provided the process which forms the dielectric thin film which consists of a compound expressed with the following general formula (1) on a semi-conductor layer, and is ABO3. .... (1)
(A is at least one sort of elements chosen from the group which consists of calcium, Ba, Sr, Pb, and La here, and B is at least one sort of elements chosen from the group which consists of Zr and Ti)
Formation of said dielectric thin film is the manufacture approach of the semiconductor device characterized by being carried out at the temperature of 1000 degrees C or less to the bottom of the pressure below 400 Torr by the chemical-vapor-deposition method using the material gas containing beta diketone complex compound of said element A, beta diketone complex compound of said element B, and an oxidizer.
[0015] this invention -- setting -- ABO3 of a general formula (1) SrTiO3 mentioned above as an example of a compound expressed, and Bax Sr1-x TiO3 and PZT -- in addition -- for example, Pb1-x Lax Zry Ti1-y O3 (0<=x<=1 and 0<=y<=1) can be mentioned.
[0016] In this invention, the raw material containing beta diketone complex compound of said element A, beta diketone complex compound of said element B, and an oxidizer is used, and it is said formula by the chemical-vapor-deposition method (CVD). ABO3 The dielectric thin film which consists of a compound expressed is formed. Thin film formation by the chemical-vapor-deposition method can be performed in a CVD process as carried out conventionally.
[0017] In the above-mentioned beta diketone complex compound used as a raw material of CVD, especially the ligand part is not limited, for example, can use the following.
[0018] - Dipivaloyl methane (DPM;C11H19O2)
In addition, naming according to IUPAC of DPM is 2, 2, 6, and 6-tetramethyl. - It is 3 and 5-heptane dione.
[0019] - Hexafluoro acetylacetone (HFA;C5 HF 6O2)
Moreover, especially an oxidizer is not limited, either and what activated these gas with the plasma or light in molecular oxygen (O2), N2 O, NO2, NO, O3, the furan (C4 H4 O) and the tetrahydrofuran (C4 H8 O), and the list can be used. From the simplicity on use, it is O2. It is used preferably and this effect of the invention can also be obtained enough. However, especially since the decomposition reaction in the gaseous phase of a raw material is controlled further and very big effectiveness can be acquired if N2 O is used, it is desirable.
[0020] Setting to this invention, the pressure and temperature of a CVD process are below 100 Torr more preferably 1000 degrees C or less below in 400 Torr. It is 700 degrees C or less. If a pressure

exceeds 400 Torr, however it may set up other process conditions, it will become difficult to control the decomposition reaction of the raw material in the inside of a gaseous phase. Moreover, shortly after reaction temperature exceeds 1000 degrees C, a raw material compound will react with a substrate. It becomes difficult to obtain the thin film of uniform thickness in any [these] case. the conditions concerning an above-mentioned pressure and temperature preferably -- the growth rate of a high dielectric thin film -- a reaction -- it sets up so that it may become rate-limiting.
[0021] In one desirable mode of this invention, said CVD process is performed at temperature lower than which pyrolysis temperature of beta diketone complex of said element A, and beta diketone complex of said element B. By this, the smooth nature of not only step coverage but a high dielectric thin film front face can be improved.
[0022] Moreover, supply of the raw material in a CVD process is controlled by other desirable modes of this invention, and in them, the amount of supply of beta diketone complex of said element B (Zr and/or Ti) is set up so that it may become 5 or more times of the amount of supply of beta diketone complex of said element A (calcium, Ba, Sr, Pb, and/or La) by the mole ratio. By this, the crystallinity of a high dielectric thin film and dielectric constant which are made into the purpose can be improved.
[0023] The two above-mentioned desirable modes may be combined in this invention.
[0024]
[Function]
(1) The most important things in this invention are using beta diketone complex compound of said element A and Element B, and performing CVD at the temperature of 1000 degrees C or less to the bottom of the pressure below 400 Torr as a metal raw material of CVD. When organic metals other than this are used as a metal raw material of CVD, or when the CVD conditions from which it separates from the above-mentioned range are used, expected good step coverage cannot be obtained.
[0025] Moreover, when the above-mentioned CVD conditions are put in another way from an operation-viewpoint, when growth of the high dielectric thin film by CVD is performed not under supply rate-limiting conditions but under reaction rate-limiting conditions, it is things. Then, this point is explained first.
[0026] Relation between the membranous growth rates and growth temperature in CVD as shown in drawing 1 is usually. That is, when a growth rate is taken along an axis of ordinate and membranous growth temperature is taken along an axis of abscissa, a certain specific temperature has membranous growth temperature and a membranous growth rate in proportionality, and a growth rate will become fixed if the specific temperature is exceeded. The reaction condition equivalent to the field which has fixed inclination by drawing 1 , i.e., the field to which membranous growth temperature and a membranous growth rate are proportional, is called reaction rate-limiting conditions. Under reaction rate-limiting conditions, since the catabolic rate of a raw material is slow, a raw material diffuses sufficient distance, before it produces a pyrolysis reaction, also after arriving at a substrate front face. Therefore, as a result of a high dielectric film's accumulating also on the part which a raw material cannot reach easily at homogeneity, thickness becomes uniform and becomes good [the step coverage on the substrate which has a level difference].
[0027] Drawing 2 is StTiO3. About the case where the film is deposited, the temperature dependence of Sr rate of sedimentation and Ti rate of sedimentation when supplying Sr raw material and Ti raw material of a constant rate to a CVD chamber is shown. This drawing shows that Sr rate of sedimentation and Ti rate of sedimentation are proportional to temperature in temperature with the skin temperature of a substrate lower than about 480 degrees C. Moreover, drawing 3 shows the same curve about the case of the PZT film. Also in this case, in the membrane formation temperature of 500 degrees C or less, each metallic element comes to fulfill reaction rate-limiting conditions.
[0028] (2) and the reactions above at time -- although it is also possible to increase the amount of supply of material gas as a means to perform CVD under rate-limiting conditions, especially a useful thing is lowering membrane formation temperature as mentioned above, and controlling disassembly of the raw material on the front face of a substrate. However, if it low-temperature-izes, although good step coverage is obtained, the smooth nature of the front face of the obtained film may get worse. For

example, if membranes are formed in such a temperature field about the element of an IIa group like Sr, Ba, and calcium, the smooth nature on the front face of a thin film will get worse remarkably. The thin film inferior to the smooth nature of such a front face is not suitable as a capacitor insulator layer of LSI.

[0029] then, an artificer etc. states below, as a result of investigating the cause -- as -- the reaction of the above [an organic metal raw material] -- it discovered that it was the cause by which a part degrades decomposition in a gaseous phase and a lifting and this degrade smooth nature under a rate-limiting condition. General formula ABO3 If the element A, i.e., the element of an IIa group like Sr and Ba, which can be set is explained, the decomposition temperature Tc peculiar to each complex exists in the DPM complex of these elements. For example, the decomposition temperature Tc in the gaseous phase of Sr (DPM)2 is as being shown in drawing 4 . In addition, Tc in this case changes like illustration depending on oxidizer conditions. Anyway, it sets to a temperature field higher than Tc, and is Sr (DPM)2. Before arriving at a substrate front face, it will decompose in a gaseous phase. Consequently, as shown in drawing 5 , it will be formed of a vapor phase cracking, the slack particle 2 will adhere to the front face of a substrate 1, and the high dielectric film 3 will accumulate by good covering nature on it. This is the cause of worsening the smooth nature on the front face of a thin film.
[0030] therefore, the desirable voice of this invention -- CVD for forming a high dielectric constant thin film, in order to set like and to prevent the vapor phase cracking of such an organic metal -- a reaction -- it not only carries out under rate-limiting conditions, but it performs CVD at temperature lower than Tc of all the organometallic compounds used as a raw material. It not only obtains good step coverage, but by this, it can improve the smooth nature of a high dielectric thin film front face. In addition, it is dependent also on conditions other than membrane formation temperature, for example, the above-mentioned decomposition temperature Tc changes also with the pressures in the membrane formation chamber at the time of membrane formation. Therefore, after **(ing) on actual membrane formation conditions and asking for the decomposition temperature Tc of each organometallic compound, membranes are formed at temperature lower than these Tc.
[0031] (3) next, still more nearly another desirable voice in this invention -- attach like and explain. In this mode, it is a mole ratio and the amount of supply of beta diketone complex of said element B (Zr and/or Ti) is controlled to become 5 or more times of the amount of supply of beta diketone complex of said element A (calcium, Ba, Sr, Pb, or La). this configuration -- membrane formation temperature -- low temperature ---izing -- a reaction -- also when performing CVD under rate-limiting conditions, the metallic element presentation in a high dielectric thin film can be made into a desirable ratio, and the quality high dielectric thin film excellent in crystallinity can be formed. The operation is explained below.
[0032] previous statement -- like -- SrTiO3 Or PbZrx Ti1-x O3 etc. -- in the high dielectric which has a perovskite crystal structure [like], only when a crystal structure takes a perovskite structure, a desired high dielectric constant can be obtained. Therefore, in order to obtain a desired high dielectric constant, it is required to control the ratio of each metallic element in these multiple oxides to less than **10% of stoichiometry, and to consider as the perovskite crystal structure. For example, the dielectric constant of strontium titanate shows a presentation dependency as shown in drawing 6 . Like illustration, if Sr/(Sr+Ti) is the stoichiometry of 0.5, about 550 dielectric constant will be obtained. However, if this ratio shifts from stoichiometry greatly and it becomes impossible to take the perovskite crystal structure, only about 30 dielectric constant will be obtained.
[0033] If strontium titanate is formed by CVD on the other hand, supplying a raw material so that Sr/(Sr+Ti) ratio in material gas may be set to 0.5, as shown in drawing 7 , Sr/(Sr+Ti) ratio in the deposition film will change depending on membrane formation temperature. Like illustration, when membrane formation temperature is 600 degrees C, Sr/(Sr+Ti) ratio in a metal oxide film are set to 0.5, and good crystallinity is acquired. However, if membrane formation temperature is reduced in order to obtain good step coverage according to this invention, the ratio of titanium will fall and good crystallinity will no longer be acquired. This phenomenon is because disassembly of a titanium raw material simple substance will be controlled and the following reactions become dominant, when the titanium raw

material and the alkaline earth metal raw material coexist in a gaseous phase at low temperature.
[0034] That is, it is Sr (DPM)2 as an alkaline earth metal raw material. It uses and is TiO (DPM)2 as a titanium raw material. When it uses, it is m-Sr (DPM)2. + TiO2 (DPM) -> Srm Ti-R[, however R are organic radicals.]
** -- a reaction [like] arises.
[0035] It is the case of m= 1 that an ideal crystal presentation is acquired. Conditions for such an ideal reaction to become dominant change with conditions, such as membrane formation temperature. the reaction which follows this invention as a result of an artificer's etc. inquiring wholeheartedly -- the ratio [on CVD in rate-limiting conditions, and as opposed to the amount of supply of an alkaline earth raw material] of the amount of supply of a titanium raw material -- a mole ratio -- the time or more of five -- the above -- it traced that an ideal reaction became dominant. In addition, the mole ratio of this amount of feeding is equal to the division ratio of each raw material.
[0036] therefore -- if the amount of supply of beta diketone complex of said element B (Zr and/or Ti) to the amount of supply of beta diketone complex of said element A (calcium, Ba, Sr, Pb, and/or La) is controlled to become 5 or more times by the mole ratio -- a reaction -- also in case a high dielectric constant thin film is formed by CVD under rate-limiting conditions, the thin film which has the good perovskite crystal structure and a desired high dielectric constant, and was excellent in insulation can be formed.
[0037]
[Example] Hereafter, the example of this invention is explained with reference to a drawing.
[0038] an example 1 -- this example -- as Sr raw material -- Sr (C11H19O2)2 as Ti raw material -- TiO (C11H19O2)2 respectively -- using -- further -- as an oxidizer -- O2 It used and the strontium titanate (SrTiO3) thin film was formed on Si substrate with chemical vapor growth with a growth temperature of 450 degrees C.
[0039] Drawing 8 is drawing showing the outline of the chemical-vapor-deposition equipment used for formation of a thin film in this example. This equipment is divided roughly, consists of a reaction container which performs chemical vapor deposition, and a supply and exhaust conductor system which performs supply and discharge of the material gas to this reaction container, an oxidizer, etc., and performs supply and discharge of various gas by accommodation of a bulb by making argon gas into carrier gas.
[0040] The gas supply system of this equipment branches to two lines from the argon gas supply line 113 linked to the source of argon gas supply which is not illustrated, one side is connected to the material gas supply pipe 114 through the mass flow rate controller 124, and another side is connected to the oxygen gas supply pipe 116 through the mass flow rate controller 126. These two networks were introduced into the piping heating oven 173, respectively, and are connected to the reaction container 101. The exhaust pipe 118 connected to a vacuum pump 107 through a pressure control valve 106 has connected with the reaction container 101. On the other hand, the exhaust pipe 115 connected to the argon gas supply line 113 through the mass flow rate controller 125 passes through the piping heating oven 173 interior, it carries out direct continuation to an exhaust pipe 118, and it is making the gas excretory system of this equipment. Two more lines have branched from the argon gas supply line 113, and one side is connected to the raw material restoration container 111 held in the raw material heating oven 171 through the mass-flow-rate controller 121 and the pressure detector 161. The network of another side is connected to the raw material restoration container 112 held in the raw material heating oven 172 through the mass-flow-rate controller 122 and the pressure detector 162. The raw material restoration container 171 is connected to the material gas supply pipe 114 with the passage change vessel 141 through a pressure control valve 151. This passage change machine 141 is connected to an exhaust pipe 115 through a bulb 131. Similarly, the raw material restoration container 172 is connected to the material gas supply pipe 114 with the passage change vessel 142 through a pressure control valve 152. This passage change machine 142 is connected to an exhaust pipe 115 through a bulb 132. By switching passage using these passage change machines 141 and 142, supply in the reaction container 101 of material gas and discharge through an exhaust pipe 115 are performed. Moreover, the oxygen gas

source of supply which is not illustrated has connected with the oxygen gas supply pipe 116 with the passage change vessel 143 through the mass flow rate controller 123. The passage change machine 143 is connected to an exhaust pipe 115 through a bulb 133. Supply of the oxygen gas to the reaction container 101 and discharge through an exhaust pipe 115 are performed by the change of the passage change machine 143 like material gas. The reaction container 101 is equipped with a gate valve 108 and the pressure detector 105, and the resistance heating heater 103 equipped with the thermocouple 104 is further formed in the interior. The substrate 102 which is going to form a thin film is laid on this resistance heating heater 103, and is heated.

[0041] Formation of a thin film was performed according to the following processes using the above chemical-vapor-deposition equipment shown in drawing 8 .

[0042] The Si substrate 102 which formed the slot first shown in drawing 9 as a reserve phase of film growth is laid on the resistance heating heater 103. Next, high grade argon gas is supplied in the reaction container 101 through a supply system, and the air inside a container is permuted. Subsequently, it is the pressure of the reaction container 101 interior, making a vacuum pump 107 **** and supervising in the pressure detector 105. It adjusts to 10 Torr. Then, high grade oxygen gas is supplied in the reaction container 101 through the mass flow rate controller 123, and the Si substrate 102 is heated at the resistance heating heater 103. A temperature up is carried out to 450 degrees C. While carrying out the temperature up of the Si substrate 102, the argon gas which adjusted the flow rate via the mass flow rate controllers 121 and 122 respectively -- 215 degrees C -- and -- Sr2 held at 110 degrees C (C11H19O2) And TiO (C11H19O2)2 As opposed to the held raw material restoration containers 111 and 112 Respectively 300 sccm It reaches. Delivery and the obtained steam are sent out to the downstream through a supply system at a rate of 30 sccm. In that case, operate the passage change machines 141 and 142, an exhaust pipe 115 is made to open piping for free passage, and the steam is emitted to the discharge side.

[0043] Thus, growth is started after preparing. That is, it is 10 Torr about the pressure in the reaction container 101 to 450 degrees C in the temperature of the Si substrate 102 again. It holds, and after making it stabilized, the passage change machines 141 and 142 are supplied to coincidence at the reaction container 101 side, a change and material gas are supplied in the reaction container 101, and growth is made to start. Growth time amount of a thin film was made into 4 hours. After growth termination, to coincidence, a change and heating according the passage change machines 141 and 142 to a heater 103 are suspended, and a substrate 102 is cooled at an exhaust pipe 115 side. While having cooled the substrate 102, oxygen gas is passed in the reaction container.

[0044] By the above process, it is thickness abbreviation. The 100nm strontium titanate thin film was obtained. the place which performed analysis by inductively-coupled-plasma emission spectrometry (the ICP method) about this thin film -- Sr/Ti=1 it is -- things were checked. Moreover, in X diffraction measurement, any peaks other than strontium titanate could not be found out, but it was checked that this thin film is a polycrystal strontium titanate thin film. Furthermore, as a result of observing the cross section of a substrate in which the thin film was formed with a scanning electron microscope, as shown in drawing 10 , it is SrTiO3 for a flat part. SrTiO3 of the thickness of a thin film 201, and the side-face part of a slot The thickness of a thin film 202 was almost the same. in addition, it is used here the reaction to which, as for the growth temperature of 450 degrees C, rate-limiting [of the growth rate] is carried out by the reaction (decomposition) of a raw material -- it is the temperature which becomes rate-limiting.

[0045] Because of a comparison, it is growth temperature so that a growth rate may serve as supply rate-limiting conditions by which rate-limiting is carried out by the amount of supply of a raw material. Except having considered as 600 degrees C, it is the same conditions as the above, and is SrTiO3. The thin film was formed. Consequently, as shown in drawing 11 , the thickness of the thin film 204 of the lateral portion of a slot was about 70% of the thickness of the thin film 203 of a flat part.

[0046] Furthermore, it is Ti (OC three H7)4 as a raw material of Ti. Using, the raw material of Sr is Sr (C11H19O2)2 like the above. It uses and is SrTiO3. The thin film was formed. In this case, they are supply rate-limiting conditions. When it was made to grow up at 600 degrees C, as shown in drawing

12 , the thin film 206 of a slot lateral portion did not grow up to be about 30% of the thin film 205 of a flat part. Moreover, they are reaction rate-limiting conditions. It grows up in the shape of [which SrO and TiO separated when it was made to grow up at 450 degrees C] an island, and is SrTiO3. A thin film was not able to be obtained.

[0047] As mentioned above, it is Sr (C11H19O2)2 as a Sr raw material. It uses and is TiO (C11H19O2) 2 as a Ti raw material. By using, it is Ti (OC three H7)4 as a Ti raw material. SrTiO3 which has the outstanding step coverage nature which cannot be obtained when it uses A thin film can be formed. Moreover, it is SrTiO3 with almost equal thickness of a flat part and thickness of a slot lateral portion by setting growth temperature as the temperature used as reaction rate-limiting conditions. A thin film can be obtained.

[0048] It is Ba (C11H19O2)2 as a raw material of example 2Ba. It uses. Moreover, as a raw material of Sr, it is Sr (C11H19O2)2. As a raw material of Ti, it is TiO (C11H19O2)2. By using, respectively and performing the same process as an example 1, it is Bax Sr1-x TiO3 on Si substrate with a level difference. The thin film was formed.

[0049] consequently, SrTiO3 the case of a thin film -- the same -- a reaction -- growth temperature which becomes rate-limiting 450 degrees C -- Bax Sr1-x TiO3 with almost equal thickness of a flat part and thickness of a slot lateral portion The thin film was able to be obtained. By ICP analysis, it was checked that 0.45 and the Ba+Sr/Ti presentation ratio of x under presentation are 1. Moreover, Ba0.45Sr0.55TiO3 obtained by performing X diffraction measurement It was checked that a thin film is the polycrystalline substance.

[0050] Moreover, without changing a raw material, by adjusting the flow rate of the carrier gas to Ba raw material container and Sr raw material container, presentation x is changed and it is Bax Sr1-x TiO3. The thin film was formed.

[0051] Consequently, in reaction rate-limiting conditions, there is nothing with respect to presentation x, and it is Bax Sr1-x TiO3 with almost equal thickness of the flat part of a substrate and thickness of a slot lateral portion. It checked that a thin film was obtained.

[0052] Based on the result of the example 3 aforementioned example 2, the dynamic random access memory cell (DRAM cel) which makes Bax Sr1-x TiO3 thin film a capacitor insulator layer was produced with the following procedures. The cross section of this DRAM cel is shown in drawing 13 .

[0053] First, the field oxide 302 for performing isolation is formed on the field (100) of the p-type silicon substrate 301. Next, gate oxide 303 is formed, and the polycrystal silicon-gate electrode 304 is continuously formed on this gate oxide. Then, the source and the drain field 305 are formed with ion-implantation, and an oxide film 306 is continuously formed as an interlayer insulation film. The above process was performed by approaches usually used in this field, such as membranous formation, patterning by the photolithography method, and ion-implantation.

[0054] Next, after forming the trench slot for a trench capacitor, the Pt film 307 used as the lower electrode of a capacitor is formed. Furthermore, it is Ba0.45Sr0.55TiO3 as a capacitor insulator layer on the Pt film 307 by the same approach as said example 2. The film 408 is formed. The thickness of the Pt lower electrode 307 is about 20nm and Ba0.45Sr0.55TiO3. The thickness of the film 408 could be 10nm. Finally, after forming the Pt film 409 in the whole surface, patterning is carried out by the photolithography method, the up electrode of a capacitor is formed, and a memory cell is completed.

[0055] thus, the substrate top which has a complicated configuration like trench structure by using the manufacture approach by this invention -- Ba0.45Sr0.55TiO3 from -- it becomes possible to form the becoming storage capacitance film in homogeneity.

[0056] Ba0.45Sr0.55TiO3 manufactured as mentioned above The memory cell which makes the film 308 a capacitor insulator layer made the conventional silicon oxide film and a conventional silicon nitride film the capacitor insulator layer, and showed the high storage capacitance of about 30 times as compared with the memory cell which has the same trench structure. This has suggested that DRAM with a degree of integration higher about 30 times than the conventional DRAM can be produced.

[0057] It removes using stack structure for an example 4 capacitor part, and is Ba0.45Sr0.55TiO3 by the same procedure as an example 3. The DRAM cel which makes the film a capacitor insulator layer was

produced. Drawing 8 shows the cross-section structure of the DRAM cel created in this example. the substrate top which has a complicated configuration like stack structure by using the manufacture approach of this invention which gave the same reference number to the same functional division as drawing 13 in this drawing -- Ba0.45Sr0.55TiO3 from -- it becomes possible to form the becoming capacitor insulator layer in homogeneity.

[0058] Ba0.45Sr0.55TiO3 manufactured as mentioned above The memory cell which makes the film 308 a capacitor insulator layer showed the high storage capacitance of about 30 times as compared with the memory cell which makes the conventional silicon oxide film and a conventional silicon nitride film a capacitor insulator layer, and has the same stack structure like the case of the trench structure of an example 3.

[0059] an example 5 -- the voice of this invention with this desirable example -- the voice which obtains the surface smooth nature which was excellent in the high dielectric constant capacitor insulator layer while like -- it is related like. That is, the CVD process in this example is performed at temperature lower than which vapor-phase-cracking temperature of the metallic compounds used for a raw material. Hereafter, with reference to drawing 15 and drawing 16 , it explains according to the manufacture process of DRAM.

[0060] (1) Form the thermal oxidation film 402 on the P type (100) single crystal silicon substrate 401 of specific resistance 10 ohm-cm, and, subsequently deposit the polish barrier layer 403 and silicon oxide 404 which consist of a silicon nitride by CVD one by one. Next, pattern NINGU of the silicon oxide 404 is carried out by the usual photo etching. By performing RIE by using this pattern 404 as a mask, the polish barrier layer 403, the thermal oxidation film 402, and a silicon substrate 401 are etched into a sequential selection target, and as shown in drawing 15 (A), the concave used as a component isolation region is formed.

[0061] (2) Next, deposit silicon oxide 405 on the whole surface by LPCVD, and bury the concave used as an isolation slot field. Subsequently, the condition of drawing 15 (B) is acquired by grinding by the chemical mechanical-polishing method and carrying out flattening of this silicon oxide 405 and the silicon oxide pattern 404 until the polish barrier layer 403 is exposed. Like illustration, silicon oxide 405 is embedded in a concave and isolation is attained.

[0062] (3) Next, exfoliate the polish barrier layer 403 and exfoliate said silicon thermal oxidation film 402 by fluoric acid etc. further. Then, the gate oxide 406 which consists of thin thermal oxidation film is formed by oxidizing a component field thermally. Subsequently, the N type polycrystalline silicon film is deposited on the whole surface by the LPCVD method, and the Guesde electrode 407 is formed by carrying out pattern NINGU of this. Furthermore, the ion implantation of the N type impurity is carried out by using the gate electrode 407 and the component demarcation membrane 405 as a blocking mask. Thereby, the source drain field 408,409 separated mutually is formed in self align. This condition is shown in drawing 15 (C).

[0063] (4) Next, form the contact hole which arrives at the source drain field 408 according to a PEP process after forming the thick CVD oxide film 410 in the whole surface as an interlayer insulation film. Then, the bit line 411 which contacted the source drain field 408 through this contact hole is formed by performing deposition and pattern NINGU of the tungsten silicide film. Subsequently, after depositing the CVD oxide film 413 as an interlayer insulation film, the contact hole which arrives at the source drain field 409 is formed by using a PEP process. Furthermore, the tungsten film 412 is embedded in this contact hole by performing selection CVD. In this way, the condition which shows in drawing 15 (D) is acquired.

[0064] (5) Next, form the silicon nitride 415 in the whole surface by plasma CVD after depositing the CVD oxide film 414 on the whole surface. Then, this CVD oxide film 414 and the silicon nitride 415 are alternatively etched by PEP until the tungsten film 412 is exposed. This forms the crevice for forming the capacitor of DRAM. Subsequently, the nitriding tungsten film 416 and the platinum film 417 are deposited on the whole surface by the spatter. Then, the platinum film 417 and the nitriding tungsten film 416 are ground, and these conductivity film 417,416 is made to remain only in said crevice by the chemical mechanical-polishing method which makes the silicon nitride 415 a polish barrier layer. In this

way, the lower electrode of a capacitor is formed and the condition which shows in drawing 16 (E) is acquired.
[0065] (6) Next, form the strontium titanate film 418 with a CVD method as a capacitor insulator layer. Then, the titanium nitride film 419 is deposited by CVD on the capacitor insulator layer 418, and pattern NINGU of this is carried out. In this way, the plate electrode 419 is formed and the condition of drawing 16 (F) is acquired.
[0066] Though natural, formation of the capacitor insulator layer 418, i.e., the strontium titanate film, is important at this process. In this example, the strontium titanate film 418 is formed as follows.
[0067] Sr2 of a raw material (DPM) And TiO2 (DPM) It supplies carrying out bubbling by Ar gas. Oxygen gas is used as an oxidizer. Sr (DPM)2 And TiO (DPM)2 the inside of a thermostat -- respectively -- 215 degrees C -- and -- It maintains at 140 degrees C. a quantity of gas flow -- carrier gas of Sr Carrier gas of 325 sccm and Ti 125 sccm and oxygen gas 50 sccm -- it is -- the total flow 500 sccm it is . Moreover, pressure at the time of membrane formation It is referred to as 10 Torr. The equipment used for this membrane formation is the same as the equipment of drawing 7 used in the example 1. Sr2 at this time (DPM) The amount of supply is 0.5 mmol/m2. It becomes. It sets on this membrane formation condition, and is Sr (DPM)2. Decomposition temperature in the inside of a gaseous phase It is 440 degrees C. Therefore, membrane formation is lower than this decomposition temperature. It carries out at 420 degrees C.
[0068] In this way, this after depositing the strontium titanate film 418 It anneals in the oxygen plasma of 400 degrees C and 0.1Torr. By this, since membranes were formed at low temperature, the carbon which remained in the film is removed. Then, said strontium titanate film 418 is crystallized by the rapid oxidizing [thermally] method for 1 minute at 700 degree C. In this way, step coverage is good and the capacitor insulator layer excellent in surface smooth nature which consists of a high dielectric thin film is obtained. Here, when AFM (atomic force microscope) estimates flat-surface smooth nature, the difference of elevation of surface irregularity 0.5 nm It was the following.
[0069] (7) After that, form the passivation film according to the usual LSI manufacture process, form required defeat, and manufacture an integrated circuit. Explanation is omitted about the detail of these processes.
[0070] an example 6 -- temperature lower than which vapor-phase-cracking temperature of the metallic compounds used for a raw material in order that this example may also obtain the surface smooth nature which was excellent in the high dielectric constant capacitor insulator layer -- a CVD process -- ****** -- it is related with a mode. Hereafter, it explains with reference to drawing 17 .
[0071] (1) Perform even the processes 1-4 of an example 5 similarly, and acquire the condition of drawing 15 (D). The subsequent process is as follows.
[0072] First, the ruthenium oxide film 501 of 1 micrometer of thickness is deposited on the CVD oxide film 413 using sputtering, and the CVD oxide film 502 is further deposited on it. Subsequently, after carrying out pattern NINGU of the CVD oxide film 502, anisotropic etching of the ruthenium oxide film 501 is carried out by RIE by using this pattern as a mask. This forms the pattern of the ruthenium oxide film 501 used as the lower electrode of a DRAM capacitor, as shown in drawing 17 (A).
[0073] (2) Next, apply the desirable mode of this invention and form the capacitor insulator layer 503 which consists of strontium titanate, after removing the CVD oxide film pattern 502. Then, the nitriding tungsten film is deposited using CVD and the plate electrode 504 which consists of nitriding tungsten film is formed by carrying out pattern NINGU of this. This condition is shown in drawing 17 (B).
[0074] The capacitor insulator layer 503 is formed as follows. Sr (DPM)2 and TiO (DPM)2 of a raw material the inside of a thermostat -- respectively -- 215 degrees C -- and -- It maintains at 140 degrees C, and it supplies in a cold wall type CVD chamber, carrying out bubbling by Ar gas. N2 O gas is used as an oxidizer. The conditions of supply and the used equipment of a raw material are the same as an example 5. Sr2 at this time (DPM) Decomposition temperature in the inside of a gaseous phase It is 460 degrees C. Therefore, membrane formation is lower than this decomposition temperature. It carries out at 440 degrees C. In this way, after depositing the strontium titanate film 418, this is set in an oxygen ambient atmosphere. It anneals for 30 minutes and is made to crystallize at 600 degrees C. In this way,

step coverage is good and the capacitor insulator layer excellent in surface smooth nature which consists of a high dielectric thin film of strontium titanate is obtained. Here, when AMF estimates flat-surface smooth nature, the difference of elevation of surface irregularity 0.2 nm It was the following.
[0075] (3) After that, form the passivation film according to the usual LSI manufacture process, form required defeat, and manufacture an integrated circuit. Explanation is omitted about the detail of these processes.
[0076] an example 7 -- the voice of this invention with this desirable example -- the voice which forms the high dielectric constant capacitor insulator layer which maintained the good perovskite crystal structure while performing CVD of reaction rate-limiting **, in order to obtain good step coverage, while like -- it is related like. That is, the CVD process in this example controls the ratio of the amount of supply of Ti raw material to the amount of supply of for example, Sr raw material by the mole ratio or more to five, and is performed.
[0077] In this example, strontium titanate is formed using the CVD system shown in drawing 18 . This equipment consists of the exhaust air system 601, a reaction container 602, and a gas supply system 603 like illustration. Moreover, as a raw material, it is Sr (DPM)2. And TiO2 (DPM) It uses and is O2 as an oxidizer. It uses.
[0078] Sr2 of a metal raw material (DPM) And TiO2 (DPM) It is contained by the raw material container 604,605 made from stainless steel, and, as for these containers, each is stored in the oven 606,607 in which temperature control is independently possible. By storing a raw material container in oven, the temperature of a raw material is extremely controllable to stability. Moreover, the pressure control valve 608,609 is formed in the outlet of the raw material container 604,605, and the pressure in each raw material container can be controlled now. Bubbling of the raw material by Ar gas performs supply of a raw material. Ar gas purified with purification equipment 610 has a flow rate controlled by the massflow controller 611,612, and carries out bubbling of the raw material in the raw material container 604,605. It is conveyed by Ar gas, it sets in the preceding paragraph of the reaction container 602, and the vaporized raw material is O2. After being mixed, it is introduced through the shower nozzle 613 in the reaction container 602. If a CVD reaction occurs into a reaction container, the thin film of strontium titanate will be formed in the substrate front face laid in the susceptor 615 held at the heater 614 at constant temperature.
[0079] The above-mentioned CVD process is performed on condition that the following, in order to realize good step coverage and the good perovskite crystal structure.
[0080] Sr2 (DPM) And TiO2 (DPM) It is each about temperature. 215 degrees C reaches. The internal pressure of the raw material container 604,605 which held at 140 degrees C and has held these raw materials is all. 100 Torr It maintains. Carrier gas flow rate of Sr Carrier gas flow rate of 300 sccm and Ti It is referred to as 35 sccm. The amount of each raw material supplied to a substrate in this condition is Sr (DPM)2. 5 mmol/m2 and TiO2 (DPM) It becomes 50 mmol/m2. in order [moreover,] to realize good step coverage -- the membrane formation rate of Sr and Ti -- a reaction -- it becomes rate-limiting -- as -- membrane formation temperature 420 degrees C and membrane formation pressure 10 Torr and the total flow 500 sccm CDV of the strontium titanate film is performed on conditions.
[0081] In this way, after forming the strontium titanate film, it is made to crystallize by performing annealing under ordinary pressure in the oxygen ambient atmosphere of 700 **. In this way, the obtained strontium titanate film has good step coverage, and, moreover, has the good perovskite crystal structure. Moreover, when the dielectric constant was evaluated using platinum as a vertical electrode, it is thickness about strontium titanate. Specific inductive capacity by the sample of 50 nm 200 Thickness At the sample of 25 nm, it is specific inductive capacity. The high value 170 was acquired.
[0082] an example 8 -- the voice in which this example as well as an example 7 forms the high dielectric constant capacitor insulator layer which maintained the good perovskite crystal structure with good step coverage -- it is related like.
[0083] In this example, strontium titanate is formed using the CVD system shown in drawing 19 . This equipment consists of the exhaust air system 701, a reaction container 702, and a gas supply system 703 like illustration. Moreover, as a raw material, it is Sr (DPM)2. And TiO2 (DPM) It used and N2 O was

used as an oxidizer.
[0084] Sr2 of a metal raw material (DPM) And TiO2 (DPM) It is in the condition of the solution which dissolved in the tetrahydrofuran, and is contained by the raw material container 104,105 made from stainless steel, respectively. Each concentration of each metal raw material in a solution is 0.01 mmol (s)/ml. The oil level of a raw material solution is pressurized using Ar, the tetrahydrofuran solution of a raw material is fed from the raw material container 704,705, and it introduces into a carburetor 708 through the liquid flow rate control unit 706,707. In addition, all piping to a carburetor 708 etc. is in the condition of a room temperature.
[0085] 250 The raw material liquid evaporated in the carburetor 708 held at ** is introduced in the reaction container 702 through the shower nozzle 713, after being conveyed by Ar gas and mixed with N2 O in the preceding paragraph of the reaction container 702. If a CVD reaction occurs into a reaction container, the thin film of strontium titanate will be formed in the substrate front face laid in the susceptor 711 held at the heater 710 at constant temperature.
[0086] The above-mentioned CVD process is performed on condition that the following, in order to realize good step coverage and the good perovskite crystal structure.
[0087] Sr2 (DPM) It is the flow rate of 0.005 sccm about a raw material solution, and the raw material solution of TiO (DPM)2 is supplied by the flow rate of 0.025 sccm. The amount of each raw material supplied to a substrate in this condition is Sr (DPM)2. 50 mmol/m2 and TiO2 (DPM) 250 mmol/m2 It becomes. Moreover, the partial pressure within a reaction container is each. 0.1 Torr And it is set to 0.5 Torr. in order to realize good step coverage on the other hand -- the membrane formation rate of Sr and Ti -- a reaction -- it becomes rate-limiting -- as -- membrane formation temperature 450 degrees C and membrane formation pressure CDV of the strontium titanate film is performed on condition that 50 Torr.

[0088] In this way, after forming the strontium titanate film, it is made to crystallize by performing annealing under ordinary pressure in the oxygen ambient atmosphere of 700 **. In this way, the obtained strontium titanate film has good step coverage, and, moreover, has the good perovskite crystal structure. Moreover, when the dielectric constant was evaluated using platinum as a vertical electrode, it is thickness about strontium titanate. At the sample of 50 nm, they are the non-dielectric constant 200 and thickness. At the sample of 25 nm, it is a non-dielectric constant. It was 170. This value is a high value equivalent to the value (K.Abe et al., J.Appl.Phys., 32, and 4186 (1993)) acquired by the conventional spatter.
[0089] As mentioned above, although the manufacture approach of the semiconductor device by this invention was explained using the example, this invention can add various modification, unless it is not limited to these examples and deviates from the essence of this invention. For example, this invention persons are N2 as carrier gas used in the case of chemical vapor deposition. And even if it is the case where helium is used, it is checking that this effect of the invention is attained. Moreover, although the C11H19O2 compound (DPM) is used as a beta diketone complex compound in the above-mentioned example, it is C5 HF 6O2 besides this. If it is beta diketone compounds of Ba, Sr, and Ti, such as a compound (HFA), it will also check that there is no change in effectiveness. Furthermore, it is O2 as an oxidizer. Also when what activated nitrogen oxides (Nx Oy) like N2 O, NO2, and NO, and O3, C4 H4 O, C4 H8 O or these gas with the plasma or light is used instead, it is checking that the same effectiveness is acquired.
[0090] Moreover, it is possible for it not to be limited to an example about any members other than a dielectric thin film, and to perform various deformation. for example, the up electrode and lower electrode of storage capacitance may not be restricted to Pt, and other metals, such as Ir, are sufficient as them -- carrying out -- PtOx and IrOx etc. -- conductive metallic oxide is sufficient and SrTiO3 which added Nb further and gave conductivity, ITO, etc. are sufficient. In the above-mentioned example, although the example which applied the manufacture approach of this invention to DRAM was explained, it is also possible to apply to semiconductor devices other than DRAM, of course.
[0091]
[Effect of the Invention] As mentioned above, according to the manufacture approach of this invention,

it is a general formula. It becomes possible to form at homogeneity the dielectric thin film which consists of a compound expressed with ABO3 (A is at least one sort of elements chosen from the group which consists of calcium, Ba, Sr, Pb, and La, and B is at least one sort of elements chosen from the group which consists of Zr and Ti) on the substrate which has a level difference. for this reason, SiO2 used conventionally and Si3 N4 etc. -- the compound 3 with a high dielectric constant, for example, SrTiO, and Bax Sr1-x TiO3 Or the semiconductor device of the high degree of integration which cannot become possible [using as storage capacitance film of the semiconductor device which has a complicated spacial configuration like a trench mold or a stack mold cel], consequently cannot obtain conventionally the dielectric thin film which consists of PZT can be obtained.

[Translation done.]

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TECHNICAL FIELD

[Industrial Application] This invention relates to the manufacture approach of a semiconductor device of having provided the capacitor, like DRAM. More specifically, it is related with the approach of forming the capacitor insulator layer (storage capacitance film) of this semiconductor device.

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PRIOR ART

[Description of the Prior Art] A capacitor is an important component in a semiconductor integrated circuit. For example, by combining a transistor and a capacitor, it consists of dynamic random access memory (DRAM) which is one sort of a semiconductor memory so that the writing and read-out of data may be performed. Moreover, also in other semiconductor integrated circuits, the capacitor is widely used as a component which accumulates a charge.
[0003] The capacitor in a semiconductor integrated circuit consists of a lower electrode which consists of a conductor on a semi-conductor substrate or this substrate, a capacitor insulator layer by which the laminating was carried out on this lower electrode, and an up electrode by which the laminating was carried out on this insulator layer. As this capacitor insulator layer, silicon oxide (SiO2) or silicon nitride (Si3 N4) is used with the conventional capacitor for integrated circuits.
[0004] By the way, it is required that the capacitor in which high integration of a semiconductor device and large capacity-ization of storage capacity followed on progressing quickly, and had big storage capacitance should be formed in a narrow plane region. Making thickness of a capacitor insulator layer thin and increasing the capacitor capacity per effective unit area as the first means which fills this demand, is performed. Moreover, as the second means, increasing the effective-surface product of a capacitor is performed by adopting three-dimensional structure. As an example of this second means, the trench capacitor technique and the SUTAKKUTO capacitor technique are known. A trench capacitor technique increases the effective area of a capacitor by forming a trench slot in a lower electrode (for example, silicon substrate), and forming a capacitor along the front face of this trench slot. Moreover, with the SUTAKKUTO capacitor technique, a big capacitor area is secured by carrying out the laminating of the one or more capacitors, and forming them on a transistor, without sacrificing a degree of integration.
[0005] However, since leakage current increases as the storage capacitance film is made thin, it is also becoming difficult technically for there to be a limit in the thin film-ization and to complicate a spacial configuration further. For this reason, as long as silicon oxide (SiO2) or silicon nitride (Si3 N4) was used as a capacitor insulator layer, it was difficult to realize DRAM with a still higher degree of integration. In fact, high integration DRAM more than a gigabit is not yet realized.
[0006] In order to attain the much more detailed-izing and high integration from such a situation, it is becoming indispensable to use the high dielectric constant ingredient with a dielectric constant higher than the conventional insulator layer as a capacitor insulator layer. Then, recent years and SiO2 Si3 N4 Using the high dielectric materials which have the crystal structure of perovskite molds, such as strontium titanate (SrTiO3) with a high dielectric constant, barium titanate strontium (Bax Sr1-x TiO3), and PZT (PbZrx Ti1-x O3), is examined. These high dielectric materials are 20 time -1,000 from silicon oxide. It has the high dielectric constant more than twice.
[0007] However, when these high dielectric materials are used for a capacitor insulator layer, there is another problem which is described below.
[0008] Generally, since these high dielectric films have small forbidden-band width of face, leakage current tends to flow at the time of electrical-potential-difference impression. For this reason, when it

thin-film-izes in order to secure a required capacitor capacity in case it is used for the capacitor of DRAM, there is a problem that leakage current becomes excessive. Moreover, since the high dielectric film which has the perovskite crystal structure has the property in which a dielectric constant falls when it is thin-film-ized, even if it thin-film-izes with much trouble, comparatively [the], the problem that capacitor capacity does not increase is. Therefore, even when using the above-mentioned high dielectric materials for a capacitor insulator layer, capacitor capacity sufficient by just it cannot be obtained, but it is necessary to use together the same spacial configuration as a trench capacitor technique and a SUTAKKUTO capacitor technique too.

[0009] When using a spacial configuration together, a high dielectric thin film must be formed by good step coverage on the front face which has irregularity. However, sputtering conventionally used for formation of the above-mentioned quantity dielectric thin film is inferior to step coverage. Therefore, in order to use a spacial configuration together, to form the above-mentioned quantity dielectric thin film not by sputtering but by the chemical vapor deposition (CVD method) excellent in step coverage is needed. However, the CVD method which can form the thin film of uniform thickness which consists of the above-mentioned high dielectric materials which are multiple oxides by good step coverage on a substrate with a level difference is not known. For this reason, it is difficult, consequently it is SiO2 to use these high dielectric thin films for a capacitor insulator layer, and to use a spacial configuration together. Si3 N4 As high in a degree of integration a semiconductor device as the semiconductor device using the storage capacitance film is not yet obtained. It will be as follows if this problem is explained more to a detail.

[0010] MOCVD which generally uses an organic metal as a raw material in case a metal oxide film is formed with a CVD method (metal organic CVD) Law is adopted. although the high dielectric materials which have the above-mentioned perovskite crystal structure are also metallic oxides, since it consists of two or more kinds of metallic oxides -- the thin film -- MOCVD -- in forming by law, there are the following problems. That is, it is indispensable for it not to be confused and to form the crystal structure of a perovskite mold, in order to obtain a thin film with a desired high dielectric constant, and in order to attain this, it is necessary to press down the gap from the stoichiometry of a crystal presentation to **10% or less. the case where precise presentation control of such multiple oxide film needs to be attained -- MOCVD -- the rate of sedimentation of a thin film -- supply -- it is carried out under the conditions which become rate-limiting. supply -- since the pyrolysis reaction of a raw material is quick under rate-limiting conditions, the alimentation proportional to the amount of supply of a raw material is obtained. Therefore, in CVD such under supply rate-limiting, the presentation of the multiple oxide to deposit is controllable to a precision by controlling the amount of supply of each raw material to a precision. Control of the amount of supply about each raw material is controllable by controlling CVD conditions, such as raw material temperature, a raw material container pressure, and a raw material bubbling quantity of gas flow, to a precision. such an approach -- Bax Sr1-x TiO3 etc. -- it is used for formation of high-temperature superconductor film, such as a dielectric thin film and YBa2 Cu3 O7-d.

[0011] however, the above supplies -- although precise presentation control becomes possible in CVD in the rate-limiting bottom, it is inferior to step coverage for the following reason. That is, under such supply rate-limiting conditions, shortly after a raw material reaches a substrate, a decomposition reaction will be caused and deposited on a substrate front face, without fully spreading. Therefore, uniform thickness cannot be obtained when the part which a raw material tends to reach like trench structure, and the part which cannot reach easily exist. Therefore, MOCVD under supply rate-limiting does not suit the purpose of using together a spacial configuration like a trench capacitor and a SUTAKKUTO capacitor, and cannot become a technique for corresponding to a gigabit generation.

[Translation done.]

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EFFECT OF THE INVENTION

[Effect of the Invention] As mentioned above, according to the manufacture approach of this invention, it is a general formula. It becomes possible to form at homogeneity the dielectric thin film which consists of a compound expressed with ABO3 (A is at least one sort of elements chosen from the group which consists of calcium, Ba, Sr, Pb, and La, and B is at least one sort of elements chosen from the group which consists of Zr and Ti) on the substrate which has a level difference. for this reason, SiO2 used conventionally and Si3 N4 etc. -- the compound 3 with a high dielectric constant, for example, SrTiO, and Bax Sr1-x TiO3 Or the semiconductor device of the high degree of integration which cannot become possible [using as storage capacitance film of the semiconductor device which has a complicated spacial configuration like a trench mold or a stack mold cel], consequently cannot obtain conventionally the dielectric thin film which consists of PZT can be obtained.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] This invention is made in view of the above-mentioned situation. The technical problem SiO2 used conventionally and Si3 N4 etc. -- the thin film of a high dielectric compound with a high dielectric constant -- Namely, in case the semiconductor device which makes thin films, such as SrTiO3, Bax Sr1-x TiO3, and PZT, a capacitor insulator layer is manufactured It is offering the approach of forming these quantities dielectric thin film by uniform thickness on a substrate, and forming by good step coverage also on the substrate which has a level difference especially. It becomes possible to become possible at the same time it uses a high dielectric thin film as a capacitor insulator layer to use together a spacial configuration like a trench capacitor and a SUTAKKUTO capacitor, as a result to manufacture a semiconductor device with a more high degree of integration by such approach.

[Translation done.]

MEANS

[Means for Solving the Problem] Even if artificers are high dielectric thin films, such as SrTiO3, Bax Sr1-x TiO3, and PZT, wholeheartedly as a result of research, while they choose a specific raw material As it fully spread, when performing CVD on the substrate front face on attainment and this front face, without a raw material decomposing in a gaseous phase, it came to complete a header and this invention for the ability of the thin film which has uniform thickness to be formed also on a substrate front face with a level difference.

[0014] Namely, the manufacture approach of the semiconductor device by this invention is the manufacture approach of a semiconductor device of having provided the process which forms the dielectric thin film which consists of a compound expressed with the following general formula (1) on a semi-conductor layer, and is ABO3. .... (1)

(A is at least one sort of elements chosen from the group which consists of calcium, Ba, Sr, Pb, and La here, and B is at least one sort of elements chosen from the group which consists of Zr and Ti)

Formation of said dielectric thin film is the manufacture approach of the semiconductor device characterized by being carried out at the temperature of 1000 degrees C or less to the bottom of the pressure below 400 Torr by the chemical-vapor-deposition method using the material gas containing beta diketone complex compound of said element A, beta diketone complex compound of said element B, and an oxidizer.

[0015] this invention -- setting -- ABO3 of a general formula (1) SrTiO3 mentioned above as an example of a compound expressed, and Bax Sr1-x TiO3 and PZT -- in addition -- for example, Pb1-x Lax Zry Ti1-y O3 (0<=x<=1 and 0<=y<=1) can be mentioned.

[0016] In this invention, the raw material containing beta diketone complex compound of said element A, beta diketone complex compound of said element B, and an oxidizer is used, and it is said formula by the chemical-vapor-deposition method (CVD). ABO3 The dielectric thin film which consists of a compound expressed is formed. Thin film formation by the chemical-vapor-deposition method can be performed in a CVD process as carried out conventionally.

[0017] In the above-mentioned beta diketone complex compound used as a raw material of CVD, especially the ligand part is not limited, for example, can use the following.

[0018] - Dipivaloyl methane (DPM;C11H19O2)

In addition, naming according to IUPAC of DPM is 2, 2, 6, and 6-tetramethyl. - It is 3 and 5-heptane dione.

[0019] - Hexafluoro acetylacetone (HFA;C5 HF 6O2)

Moreover, especially an oxidizer is not limited, either and what activated these gas with the plasma or light in molecular oxygen (O2), N2 O, NO2, NO, O3, the furan (C4 H4 O) and the tetrahydrofuran (C4 H8 O), and the list can be used. From the simplicity on use, it is O2. It is used preferably and this effect of the invention can also be obtained enough. However, especially since the decomposition reaction in the gaseous phase of a raw material is controlled further and very big effectiveness can be acquired if N2 O is used, it is desirable.

[0020] Setting to this invention, the pressure and temperature of a CVD process are below 100 Torr

more preferably 1000 degrees C or less below in 400 Torr. It is 700 degrees C or less. If a pressure exceeds 400 Torr, however it may set up other process conditions, it will become difficult to control the decomposition reaction of the raw material in the inside of a gaseous phase. Moreover, shortly after reaction temperature exceeds 1000 degrees C, a raw material compound will react with a substrate. It becomes difficult to obtain the thin film of uniform thickness in any [these] case. the conditions concerning an above-mentioned pressure and temperature preferably -- the growth rate of a high dielectric thin film -- a reaction -- it sets up so that it may become rate-limiting.

[0021] In one desirable mode of this invention, said CVD process is performed at temperature lower than which pyrolysis temperature of beta diketone complex of said element A, and beta diketone complex of said element B. By this, the smooth nature of not only step coverage but a high dielectric thin film front face can be improved.

[0022] Moreover, supply of the raw material in a CVD process is controlled by other desirable modes of this invention, and in them, the amount of supply of beta diketone complex of said element B (Zr and/or Ti) is set up so that it may become 5 or more times of the amount of supply of beta diketone complex of said element A (calcium, Ba, Sr, Pb, and/or La) by the mole ratio. By this, the crystallinity of a high dielectric thin film and dielectric constant which are made into the purpose can be improved.

[0023] The two above-mentioned desirable modes may be combined in this invention.

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OPERATION

[Function]
(1) The most important things in this invention are using beta diketone complex compound of said element A and Element B, and performing CVD at the temperature of 1000 degrees C or less to the bottom of the pressure below 400 Torr as a metal raw material of CVD. When organic metals other than this are used as a metal raw material of CVD, or when the CVD conditions from which it separates from the above-mentioned range are used, expected good step coverage cannot be obtained.
[0025] Moreover, when the above-mentioned CVD conditions are put in another way from an operation-viewpoint, when growth of the high dielectric thin film by CVD is performed not under supply rate-limiting conditions but under reaction rate-limiting conditions, it is things. Then, this point is explained first.
[0026] Relation between the membranous growth rates and growth temperature in CVD as shown in drawing 1 is usually. That is, when a growth rate is taken along an axis of ordinate and membranous growth temperature is taken along an axis of abscissa, a certain specific temperature has membranous growth temperature and a membranous growth rate in proportionality, and a growth rate will become fixed if the specific temperature is exceeded. The reaction condition equivalent to the field which has fixed inclination by drawing 1 , i.e., the field to which membranous growth temperature and a membranous growth rate are proportional, is called reaction rate-limiting conditions. Under reaction rate-limiting conditions, since the catabolic rate of a raw material is slow, a raw material diffuses sufficient distance, before it produces a pyrolysis reaction, also after arriving at a substrate front face. Therefore, as a result of a high dielectric film's accumulating also on the part which a raw material cannot reach easily at homogeneity, thickness becomes uniform and becomes good [the step coverage on the substrate which has a level difference].
[0027] Drawing 2 is StTiO3. About the case where the film is deposited, the temperature dependence of Sr rate of sedimentation and Ti rate of sedimentation when supplying Sr raw material and Ti raw material of a constant rate to a CVD chamber is shown. This drawing shows that Sr rate of sedimentation and Ti rate of sedimentation are proportional to temperature in temperature with the skin temperature of a substrate lower than about 480 degrees C. Moreover, drawing 3 shows the same curve about the case of the PZT film. Also in this case, in the membrane formation temperature of 500 degrees C or less, each metallic element comes to fulfill reaction rate-limiting conditions.
[0028] (2) and the reactions above at time -- although it is also possible to increase the amount of supply of material gas as a means to perform CVD under rate-limiting conditions, especially a useful thing is lowering membrane formation temperature as mentioned above, and controlling disassembly of the raw material on the front face of a substrate. However, if it low-temperature-izes, although good step coverage is obtained, the smooth nature of the front face of the obtained film may get worse. For example, if membranes are formed in such a temperature field about the element of an IIa group like Sr, Ba, and calcium, the smooth nature on the front face of a thin film will get worse remarkably. The thin film inferior to the smooth nature of such a front face is not suitable as a capacitor insulator layer of LSI.

[0029] then, an artificer etc. states below, as a result of investigating the cause -- as – the reaction of the above [an organic metal raw material] -- it discovered that it was the cause by which a part degrades decomposition in a gaseous phase and a lifting and this degrade smooth nature under a rate-limiting condition. General formula ABO3 If the element A, i.e., the element of an IIa group like Sr and Ba, which can be set is explained, the decomposition temperature Tc peculiar to each complex exists in the DPM complex of these elements. For example, the decomposition temperature Tc in the gaseous phase of Sr (DPM)2 is as being shown in drawing 4 . In addition, Tc in this case changes like illustration depending on oxidizer conditions. Anyway, it sets to a temperature field higher than Tc, and is Sr (DPM)2. Before arriving at a substrate front face, it will decompose in a gaseous phase. Consequently, as shown in drawing 5 , it will be formed of a vapor phase cracking, the slack particle 2 will adhere to the front face of a substrate 1, and the high dielectric film 3 will accumulate by good covering nature on it. This is the cause of worsening the smooth nature on the front face of a thin film.
[0030] therefore, the desirable voice of this invention -- CVD for forming a high dielectric constant thin film, in order to set like and to prevent the vapor phase cracking of such an organic metal -- a reaction -- it not only carries out under rate-limiting conditions, but it performs CVD at temperature lower than Tc of all the organometallic compounds used as a raw material. It not only obtains good step coverage, but by this, it can improve the smooth nature of a high dielectric thin film front face. In addition, it is dependent also on conditions other than membrane formation temperature, for example, the above-mentioned decomposition temperature Tc changes also with the pressures in the membrane formation chamber at the time of membrane formation. Therefore, after **(ing) on actual membrane formation conditions and asking for the decomposition temperature Tc of each organometallic compound, membranes are formed at temperature lower than these Tc.
[0031] (3) next, still more nearly another desirable voice in this invention -- attach like and explain. In this mode, it is a mole ratio and the amount of supply of beta diketone complex of said element B (Zr and/or Ti) is controlled to become 5 or more times of the amount of supply of beta diketone complex of said element A (calcium, Ba, Sr, Pb, or La). this configuration -- membrane formation temperature -- low temperature ---izing -- a reaction -- also when performing CVD under rate-limiting conditions, the metallic element presentation in a high dielectric thin film can be made into a desirable ratio, and the quality high dielectric thin film excellent in crystallinity can be formed. The operation is explained below.
[0032] previous statement -- like -- SrTiO3 Or PbZrx Ti1-x O3 etc. -- in the high dielectric which has a perovskite crystal structure [like], only when a crystal structure takes a perovskite structure, a desired high dielectric constant can be obtained. Therefore, in order to obtain a desired high dielectric constant, it is required to control the ratio of each metallic element in these multiple oxides to less than **10% of stoichiometry, and to consider as the perovskite crystal structure. For example, the dielectric constant of strontium titanate shows a presentation dependency as shown in drawing 6 . Like illustration, if Sr/(Sr+Ti) is the stoichiometry of 0.5, about 550 dielectric constant will be obtained. However, if this ratio shifts from stoichiometry greatly and it becomes impossible to take the perovskite crystal structure, only about 30 dielectric constant will be obtained.
[0033] If strontium titanate is formed by CVD on the other hand, supplying a raw material so that Sr/(Sr+Ti) ratio in material gas may be set to 0.5, as shown in drawing 7 , Sr/(Sr+Ti) ratio in the deposition film will change depending on membrane formation temperature. Like illustration, when membrane formation temperature is 600 degrees C, Sr/(Sr+Ti) ratio in a metal oxide film are set to 0.5, and good crystallinity is acquired. However, if membrane formation temperature is reduced in order to obtain good step coverage according to this invention, the ratio of titanium will fall and good crystallinity will no longer be acquired. This phenomenon is because disassembly of a titanium raw material simple substance will be controlled and the following reactions become dominant, when the titanium raw material and the alkaline earth metal raw material coexist in a gaseous phase at low temperature.
[0034] That is, it is Sr (DPM)2 as an alkaline earth metal raw material. It uses and is TiO (DPM)2 as a titanium raw material. When it uses, it is m-Sr (DPM)2. + TiO2 (DPM) -> Srm Ti-R[, however R are organic radicals.]

** -- a reaction [like] arises.
[0035] It is the case of m= 1 that an ideal crystal presentation is acquired. Conditions for such an ideal reaction to become dominant change with conditions, such as membrane formation temperature. the reaction which follows this invention as a result of an artificer's etc. inquiring wholeheartedly -- the ratio [on CVD in rate-limiting conditions, and as opposed to the amount of supply of an alkaline earth raw material] of the amount of supply of a titanium raw material -- a mole ratio -- the time or more of five -- the above -- it traced that an ideal reaction became dominant. In addition, the mole ratio of this amount of feeding is equal to the division ratio of each raw material.
[0036] therefore -- if the amount of supply of beta diketone complex of said element B (Zr and/or Ti) to the amount of supply of beta diketone complex of said element A (calcium, Ba, Sr, Pb, and/or La) is controlled to become 5 or more times by the mole ratio -- a reaction -- also in case a high dielectric constant thin film is formed by CVD under rate-limiting conditions, the thin film which has the good perovskite crystal structure and a desired high dielectric constant, and was excellent in insulation can be formed.

[Translation done.]

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EXAMPLE

[Example] Hereafter, the example of this invention is explained with reference to a drawing.
[0038] an example 1 -- this example -- as Sr raw material -- Sr (C11H19O2)2 as Ti raw material -- TiO (C11H19O2)2 respectively -- using -- further -- as an oxidizer -- O2 It used and the strontium titanate (SrTiO3) thin film was formed on Si substrate with chemical vapor growth with a growth temperature of 450 degrees C.
[0039] Drawing 8 is drawing showing the outline of the chemical-vapor-deposition equipment used for formation of a thin film in this example. This equipment is divided roughly, consists of a reaction container which performs chemical vapor deposition, and a supply and exhaust conductor system which performs supply and discharge of the material gas to this reaction container, an oxidizer, etc., and performs supply and discharge of various gas by accommodation of a bulb by making argon gas into carrier gas.
[0040] The gas supply system of this equipment branches to two lines from the argon gas supply line 113 linked to the source of argon gas supply which is not illustrated, one side is connected to the material gas supply pipe 114 through the mass flow rate controller 124, and another side is connected to the oxygen gas supply pipe 116 through the mass flow rate controller 126. These two networks were introduced into the piping heating oven 173, respectively, and are connected to the reaction container 101. The exhaust pipe 118 connected to a vacuum pump 107 through a pressure control valve 106 has connected with the reaction container 101. On the other hand, the exhaust pipe 115 connected to the argon gas supply line 113 through the mass flow rate controller 125 passes through the piping heating oven 173 interior, it carries out direct continuation to an exhaust pipe 118, and it is making the gas excretory system of this equipment. Two more lines have branched from the argon gas supply line 113, and one side is connected to the raw material restoration container 111 held in the raw material heating oven 171 through the mass-flow-rate controller 121 and the pressure detector 161. The network of another side is connected to the raw material restoration container 112 held in the raw material heating oven 172 through the mass-flow-rate controller 122 and the pressure detector 162. The raw material restoration container 171 is connected to the material gas supply pipe 114 with the passage change vessel 141 through a pressure control valve 151. This passage change machine 141 is connected to an exhaust pipe 115 through a bulb 131. Similarly, the raw material restoration container 172 is connected to the material gas supply pipe 114 with the passage change vessel 142 through a pressure control valve 152. This passage change machine 142 is connected to an exhaust pipe 115 through a bulb 132. By switching passage using these passage change machines 141 and 142, supply in the reaction container 101 of material gas and discharge through an exhaust pipe 115 are performed. Moreover, the oxygen gas source of supply which is not illustrated has connected with the oxygen gas supply pipe 116 with the passage change vessel 143 through the mass flow rate controller 123. The passage change machine 143 is connected to an exhaust pipe 115 through a bulb 133. Supply of the oxygen gas to the reaction container 101 and discharge through an exhaust pipe 115 are performed by the change of the passage change machine 143 like material gas. The reaction container 101 is equipped with a gate valve 108 and the pressure detector 105, and the resistance heating heater 103 equipped with the thermocouple 104 is

further formed in the interior. The substrate 102 which is going to form a thin film is laid on this resistance heating heater 103, and is heated.
[0041] Formation of a thin film was performed according to the following processes using the above chemical-vapor-deposition equipment shown in drawing 8 .
[0042] The Si substrate 102 which formed the slot first shown in drawing 9 as a reserve phase of film growth is laid on the resistance heating heater 103. Next, high grade argon gas is supplied in the reaction container 101 through a supply system, and the air inside a container is permuted. Subsequently, it is the pressure of the reaction container 101 interior, making a vacuum pump 107 **** and supervising in the pressure detector 105. It adjusts to 10 Torr. Then, high grade oxygen gas is supplied in the reaction container 101 through the mass flow rate controller 123, and the Si substrate 102 is heated at the resistance heating heater 103. A temperature up is carried out to 450 degrees C. While carrying out the temperature up of the Si substrate 102, the argon gas which adjusted the flow rate via the mass flow rate controllers 121 and 122 respectively -- 215 degrees C -- and -- Sr2 held at 110 degrees C (C11H19O2) And TiO (C11H19O2)2 As opposed to the held raw material restoration containers 111 and 112 Respectively 300 sccm It reaches. Delivery and the obtained steam are sent out to the downstream through a supply system at a rate of 30 sccm. In that case, operate the passage change machines 141 and 142, an exhaust pipe 115 is made to open piping for free passage, and the steam is emitted to the discharge side.
[0043] Thus, growth is started after preparing. That is, it is 10 Torr about the pressure in the reaction container 101 to 450 degrees C in the temperature of the Si substrate 102 again. It holds, and after making it stabilized, the passage change machines 141 and 142 are supplied to coincidence at the reaction container 101 side, a change and material gas are supplied in the reaction container 101, and growth is made to start. Growth time amount of a thin film was made into 4 hours. After growth termination, to coincidence, a change and heating according the passage change machines 141 and 142 to a heater 103 are suspended, and a substrate 102 is cooled at an exhaust pipe 115 side. While having cooled the substrate 102, oxygen gas is passed in the reaction container.
[0044] By the above process, it is thickness abbreviation. The 100nm strontium titanate thin film was obtained. the place which performed analysis by inductively-coupled-plasma emission spectrometry (the ICP method) about this thin film -- Sr/Ti=1 it is -- things were checked. Moreover, in X diffraction measurement, any peaks other than strontium titanate could not be found out, but it was checked that this thin film is a polycrystal strontium titanate thin film. Furthermore, as a result of observing the cross section of a substrate in which the thin film was formed with a scanning electron microscope, as shown in drawing 10 , it is SrTiO3 for a flat part. SrTiO3 of the thickness of a thin film 201, and the side-face part of a slot The thickness of a thin film 202 was almost the same. in addition, it is used here the reaction to which, as for the growth temperature of 450 degrees C, rate-limiting [of the growth rate] is carried out by the reaction (decomposition) of a raw material -- it is the temperature which becomes rate-limiting.
[0045] Because of a comparison, it is growth temperature so that a growth rate may serve as supply rate-limiting conditions by which rate-limiting is carried out by the amount of supply of a raw material. Except having considered as 600 degrees C, it is the same conditions as the above, and is SrTiO3. The thin film was formed. Consequently, as shown in drawing 11 , the thickness of the thin film 204 of the lateral portion of a slot was about 70% of the thickness of the thin film 203 of a flat part.
[0046] Furthermore, it is Ti (OC three H7)4 as a raw material of Ti. Using, the raw material of Sr is Sr (C11H19O2)2 like the above. It uses and is SrTiO3. The thin film was formed. In this case, they are supply rate-limiting conditions. When it was made to grow up at 600 degrees C, as shown in drawing 12 , the thin film 206 of a slot lateral portion did not grow up to be about 30% of the thin film 205 of a flat part. Moreover, they are reaction rate-limiting conditions. It grows up in the shape of [which SrO and TiO separated when it was made to grow up at 450 degrees C] an island, and is SrTiO3. A thin film was not able to be obtained.
[0047] As mentioned above, it is Sr (C11H19O2)2 as a Sr raw material. It uses and is TiO (C11H19O2) 2 as a Ti raw material. By using, it is Ti (OC three H7)4 as a Ti raw material. SrTiO3 which has the

outstanding step coverage nature which cannot be obtained when it uses A thin film can be formed. Moreover, it is SrTiO3 with almost equal thickness of a flat part and thickness of a slot lateral portion by setting growth temperature as the temperature used as reaction rate-limiting conditions. A thin film can be obtained.

[0048] It is Ba (C11H19O2)2 as a raw material of example 2Ba. It uses. Moreover, as a raw material of Sr, it is Sr (C11H19O2)2. As a raw material of Ti, it is TiO (C11H19O2)2. By using, respectively and performing the same process as an example 1, it is Bax Sr1-x TiO3 on Si substrate with a level difference. The thin film was formed.

[0049] consequently, SrTiO3 the case of a thin film -- the same -- a reaction -- growth temperature which becomes rate-limiting 450 degrees C -- Bax Sr1-x TiO3 with almost equal thickness of a flat part and thickness of a slot lateral portion The thin film was able to be obtained. By ICP analysis, it was checked that 0.45 and the Ba+Sr/Ti presentation ratio of x under presentation are 1. Moreover, Ba0.45Sr0.55TiO3 obtained by performing X diffraction measurement It was checked that a thin film is the polycrystalline substance.

[0050] Moreover, without changing a raw material, by adjusting the flow rate of the carrier gas to Ba raw material container and Sr raw material container, presentation x is changed and it is Bax Sr1-x TiO3. The thin film was formed.

[0051] Consequently, in reaction rate-limiting conditions, there is nothing with respect to presentation x, and it is Bax Sr1-x TiO3 with almost equal thickness of the flat part of a substrate and thickness of a slot lateral portion. It checked that a thin film was obtained.

[0052] Based on the result of the example 3 aforementioned example 2, the dynamic random access memory cell (DRAM cel) which makes Bax Sr1-x TiO3 thin film a capacitor insulator layer was produced with the following procedures. The cross section of this DRAM cel is shown in drawing 13 .

[0053] First, the field oxide 302 for performing isolation is formed on the field (100) of the p-type silicon substrate 301. Next, gate oxide 303 is formed, and the polycrystal silicon-gate electrode 304 is continuously formed on this gate oxide. Then, the source and the drain field 305 are formed with ion-implantation, and an oxide film 306 is continuously formed as an interlayer insulation film. The above process was performed by approaches usually used in this field, such as membranous formation, patterning by the photolithography method, and ion-implantation.

[0054] Next, after forming the trench slot for a trench capacitor, the Pt film 307 used as the lower electrode of a capacitor is formed. Furthermore, it is Ba0.45Sr0.55TiO3 as a capacitor insulator layer on the Pt film 307 by the same approach as said example 2. The film 408 is formed. The thickness of the Pt lower electrode 307 is about 20nm and Ba0.45Sr0.55TiO3. The thickness of the film 408 could be 10nm. Finally, after forming the Pt film 409 in the whole surface, patterning is carried out by the photolithography method, the up electrode of a capacitor is formed, and a memory cell is completed.

[0055] thus, the substrate top which has a complicated configuration like trench structure by using the manufacture approach by this invention -- Ba0.45Sr0.55TiO3 from -- it becomes possible to form the becoming storage capacitance film in homogeneity.

[0056] Ba0.45Sr0.55TiO3 manufactured as mentioned above The memory cell which makes the film 308 a capacitor insulator layer made the conventional silicon oxide film and a conventional silicon nitride film the capacitor insulator layer, and showed the high storage capacitance of about 30 times as compared with the memory cell which has the same trench structure. This has suggested that DRAM with a degree of integration higher about 30 times than the conventional DRAM can be produced.

[0057] It removes using stack structure for an example 4 capacitor part, and is Ba0.45Sr0.55TiO3 by the same procedure as an example 3. The DRAM cel which makes the film a capacitor insulator layer was produced. Drawing 8 shows the cross-section structure of the DRAM cel created in this example. the substrate top which has a complicated configuration like stack structure by using the manufacture approach of this invention which gave the same reference number to the same functional division as drawing 13 in this drawing -- Ba0.45Sr0.55TiO3 from -- it becomes possible to form the becoming capacitor insulator layer in homogeneity.

[0058] Ba0.45Sr0.55TiO3 manufactured as mentioned above The memory cell which makes the film

308 a capacitor insulator layer showed the high storage capacitance of about 30 times as compared with the memory cell which makes the conventional silicon oxide film and a conventional silicon nitride film a capacitor insulator layer, and has the same stack structure like the case of the trench structure of an example 3.

[0059] an example 5 -- the voice of this invention with this desirable example -- the voice which obtains the surface smooth nature which was excellent in the high dielectric constant capacitor insulator layer while like -- it is related like. That is, the CVD process in this example is performed at temperature lower than which vapor-phase-cracking temperature of the metallic compounds used for a raw material. Hereafter, with reference to drawing 15 and drawing 16 , it explains according to the manufacture process of DRAM.

[0060] (1) Form the thermal oxidation film 402 on the P type (100) single crystal silicon substrate 401 of specific resistance 10 ohm-cm, and, subsequently deposit the polish barrier layer 403 and silicon oxide 404 which consist of a silicon nitride by CVD one by one. Next, pattern NINGU of the silicon oxide 404 is carried out by the usual photo etching. By performing RIE by using this pattern 404 as a mask, the polish barrier layer 403, the thermal oxidation film 402, and a silicon substrate 401 are etched into a sequential selection target, and as shown in drawing 15 (A), the concave used as a component isolation region is formed.

[0061] (2) Next, deposit silicon oxide 405 on the whole surface by LPCVD, and bury the concave used as an isolation slot field. Subsequently, the condition of drawing 15 (B) is acquired by grinding by the chemical mechanical-polishing method and carrying out flattening of this silicon oxide 405 and the silicon oxide pattern 404 until the polish barrier layer 403 is exposed. Like illustration, silicon oxide 405 is embedded in a concave and isolation is attained.

[0062] (3) Next, exfoliate the polish barrier layer 403 and exfoliate said silicon thermal oxidation film 402 by fluoric acid etc. further. Then, the gate oxide 406 which consists of thin thermal oxidation film is formed by oxidizing a component field thermally. Subsequently, the N type polycrystalline silicon film is deposited on the whole surface by the LPCVD method, and the Guesde electrode 407 is formed by carrying out pattern NINGU of this. Furthermore, the ion implantation of the N type impurity is carried out by using the gate electrode 407 and the component demarcation membrane 405 as a blocking mask. Thereby, the source drain field 408,409 separated mutually is formed in self align. This condition is shown in drawing 15 (C).

[0063] (4) Next, form the contact hole which arrives at the source drain field 408 according to a PEP process after forming the thick CVD oxide film 410 in the whole surface as an interlayer insulation film. Then, the bit line 411 which contacted the source drain field 408 through this contact hole is formed by performing deposition and pattern NINGU of the tungsten silicide film. Subsequently, after depositing the CVD oxide film 413 as an interlayer insulation film, the contact hole which arrives at the source drain field 409 is formed by using a PEP process. Furthermore, the tungsten film 412 is embedded in this contact hole by performing selection CVD. In this way, the condition which shows in drawing 15 (D) is acquired.

[0064] (5) Next, form the silicon nitride 415 in the whole surface by plasma CVD after depositing the CVD oxide film 414 on the whole surface. Then, this CVD oxide film 414 and the silicon nitride 415 are alternatively etched by PEP until the tungsten film 412 is exposed. This forms the crevice for forming the capacitor of DRAM. Subsequently, the nitriding tungsten film 416 and the platinum film 417 are deposited on the whole surface by the spatter. Then, the platinum film 417 and the nitriding tungsten film 416 are ground, and these conductivity film 417,416 is made to remain only in said crevice by the chemical mechanical-polishing method which makes the silicon nitride 415 a polish barrier layer. In this way, the lower electrode of a capacitor is formed and the condition which shows in drawing 16 (E) is acquired.

[0065] (6) Next, form the strontium titanate film 418 with a CVD method as a capacitor insulator layer. Then, the titanium nitride film 419 is deposited by CVD on the capacitor insulator layer 418, and pattern NINGU of this is carried out. In this way, the plate electrode 419 is formed and the condition of drawing 16 (F) is acquired.

[0066] Though natural, formation of the capacitor insulator layer 418, i.e., the strontium titanate film, is important at this process. In this example, the strontium titanate film 418 is formed as follows.
[0067] Sr2 of a raw material (DPM) And TiO2 (DPM) It supplies carrying out bubbling by Ar gas. Oxygen gas is used as an oxidizer. Sr (DPM)2 And TiO (DPM)2 the inside of a thermostat -- respectively -- 215 degrees C -- and -- It maintains at 140 degrees C. a quantity of gas flow -- carrier gas of Sr Carrier gas of 325 sccm and Ti 125 sccm and oxygen gas 50 sccm -- it is -- the total flow 500 sccm it is . Moreover, pressure at the time of membrane formation It is referred to as 10 Torr. The equipment used for this membrane formation is the same as the equipment of drawing 7 used in the example 1. Sr2 at this time (DPM) The amount of supply is 0.5 mmol/m2. It becomes. It sets on this membrane formation condition, and is Sr (DPM)2. Decomposition temperature in the inside of a gaseous phase It is 440 degrees C. Therefore, membrane formation is lower than this decomposition temperature. It carries out at 420 degrees C.
[0068] In this way, this after depositing the strontium titanate film 418 It anneals in the oxygen plasma of 400 degrees C and 0.1Torr. By this, since membranes were formed at low temperature, the carbon which remained in the film is removed. Then, said strontium titanate film 418 is crystallized by the rapid oxidizing [thermally] method for 1 minute at 700 degree C. In this way, step coverage is good and the capacitor insulator layer excellent in surface smooth nature which consists of a high dielectric thin film is obtained. Here, when AFM (atomic force microscope) estimates flat-surface smooth nature, the difference of elevation of surface irregularity 0.5 nm It was the following.
[0069] (7) After that, form the passivation film according to the usual LSI manufacture process, form required defeat, and manufacture an integrated circuit. Explanation is omitted about the detail of these processes.
[0070] an example 6 -- temperature lower than which vapor-phase-cracking temperature of the metallic compounds used for a raw material in order that this example may also obtain the surface smooth nature which was excellent in the high dielectric constant capacitor insulator layer -- a CVD process -- ****** -- it is related with a mode. Hereafter, it explains with reference to drawing 17 .
[0071] (1) Perform even the processes 1-4 of an example 5 similarly, and acquire the condition of drawing 15 (D). The subsequent process is as follows.
[0072] First, the ruthenium oxide film 501 of 1 micrometer of thickness is deposited on the CVD oxide film 413 using sputtering, and the CVD oxide film 502 is further deposited on it. Subsequently, after carrying out pattern NINGU of the CVD oxide film 502, anisotropic etching of the ruthenium oxide film 501 is carried out by RIE by using this pattern as a mask. This forms the pattern of the ruthenium oxide film 501 used as the lower electrode of a DRAM capacitor, as shown in drawing 17 (A).
[0073] (2) Next, apply the desirable mode of this invention and form the capacitor insulator layer 503 which consists of strontium titanate, after removing the CVD oxide film pattern 502. Then, the nitriding tungsten film is deposited using CVD and the plate electrode 504 which consists of nitriding tungsten film is formed by carrying out pattern NINGU of this. This condition is shown in drawing 17 (B).
[0074] The capacitor insulator layer 503 is formed as follows. Sr (DPM)2 and TiO (DPM)2 of a raw material the inside of a thermostat -- respectively -- 215 degrees C -- and -- It maintains at 140 degrees C, and it supplies in a cold wall type CVD chamber, carrying out bubbling by Ar gas. N2 O gas is used as an oxidizer. The conditions of supply and the used equipment of a raw material are the same as an example 5. Sr2 at this time (DPM) Decomposition temperature in the inside of a gaseous phase It is 460 degrees C. Therefore, membrane formation is lower than this decomposition temperature. It carries out at 440 degrees C. In this way, after depositing the strontium titanate film 418, this is set in an oxygen ambient atmosphere. It anneals for 30 minutes and is made to crystallize at 600 degrees C. In this way, step coverage is good and the capacitor insulator layer excellent in surface smooth nature which consists of a high dielectric thin film of strontium titanate is obtained. Here, when AMF estimates flat-surface smooth nature, the difference of elevation of surface irregularity 0.2 nm It was the following.
[0075] (3) After that, form the passivation film according to the usual LSI manufacture process, form required defeat, and manufacture an integrated circuit. Explanation is omitted about the detail of these processes.

[0076] an example 7 -- the voice of this invention with this desirable example -- the voice which forms the high dielectric constant capacitor insulator layer which maintained the good perovskite crystal structure while performing CVD of reaction rate-limiting **, in order to obtain good step coverage, while like -- it is related like. That is, the CVD process in this example controls the ratio of the amount of supply of Ti raw material to the amount of supply of for example, Sr raw material by the mole ratio or more to five, and is performed.
[0077] In this example, strontium titanate is formed using the CVD system shown in drawing 18 . This equipment consists of the exhaust air system 601, a reaction container 602, and a gas supply system 603 like illustration. Moreover, as a raw material, it is Sr (DPM)2. And TiO2 (DPM) It uses and is O2 as an oxidizer. It uses.
[0078] Sr2 of a metal raw material (DPM) And TiO2 (DPM) It is contained by the raw material container 604,605 made from stainless steel, and, as for these containers, each is stored in the oven 606,607 in which temperature control is independently possible. By storing a raw material container in oven, the temperature of a raw material is extremely controllable to stability. Moreover, the pressure control valve 608,609 is formed in the outlet of the raw material container 604,605, and the pressure in each raw material container can be controlled now. Bubbling of the raw material by Ar gas performs supply of a raw material. Ar gas purified with purification equipment 610 has a flow rate controlled by the massflow controller 611,612, and carries out bubbling of the raw material in the raw material container 604,605. It is conveyed by Ar gas, it sets in the preceding paragraph of the reaction container 602, and the vaporized raw material is O2. After being mixed, it is introduced through the shower nozzle 613 in the reaction container 602. If a CVD reaction occurs into a reaction container, the thin film of strontium titanate will be formed in the substrate front face laid in the susceptor 615 held at the heater 614 at constant temperature.
[0079] The above-mentioned CVD process is performed on condition that the following, in order to realize good step coverage and the good perovskite crystal structure.
[0080] Sr2 (DPM) And TiO2 (DPM) It is each about temperature. 215 degrees C reaches. The internal pressure of the raw material container 604,605 which held at 140 degrees C and has held these raw materials is all. 100 Torr It maintains. Carrier gas flow rate of Sr Carrier gas flow rate of 300 sccm and Ti It is referred to as 35 sccm. The amount of each raw material supplied to a substrate in this condition is Sr (DPM)2. 5 mmol/m2 and TiO2 (DPM) It becomes 50 mmol/m2. in order [moreover,] to realize good step coverage -- the membrane formation rate of Sr and Ti -- a reaction -- it becomes rate-limiting -- as -- membrane formation temperature 420 degrees C and membrane formation pressure 10 Torr and the total flow 500 sccm CDV of the strontium titanate film is performed on conditions.
[0081] In this way, after forming the strontium titanate film, it is made to crystallize by performing annealing under ordinary pressure in the oxygen ambient atmosphere of 700 **. In this way, the obtained strontium titanate film has good step coverage, and, moreover, has the good perovskite crystal structure. Moreover, when the dielectric constant was evaluated using platinum as a vertical electrode, it is thickness about strontium titanate. Specific inductive capacity by the sample of 50 nm 200 Thickness At the sample of 25 nm, it is specific inductive capacity. The high value 170 was acquired.
[0082] an example 8 -- the voice in which this example as well as an example 7 forms the high dielectric constant capacitor insulator layer which maintained the good perovskite crystal structure with good step coverage -- it is related like.
[0083] In this example, strontium titanate is formed using the CVD system shown in drawing 19 . This equipment consists of the exhaust air system 701, a reaction container 702, and a gas supply system 703 like illustration. Moreover, as a raw material, it is Sr (DPM)2. And TiO2 (DPM) It used and N2 O was used as an oxidizer.
[0084] Sr2 of a metal raw material (DPM) And TiO2 (DPM) It is in the condition of the solution which dissolved in the tetrahydrofuran, and is contained by the raw material container 104,105 made from stainless steel, respectively. Each concentration of each metal raw material in a solution is 0.01 mmol (s)/ml. The oil level of a raw material solution is pressurized using Ar, the tetrahydrofuran solution of a raw material is fed from the raw material container 704,705, and it introduces into a carburetor 708

through the liquid flow rate control unit 706,707. In addition, all piping to a carburetor 708 etc. is in the condition of a room temperature.
[0085] 250 The raw material liquid evaporated in the carburetor 708 held at ** is introduced in the reaction container 702 through the shower nozzle 713, after being conveyed by Ar gas and mixed with N2 O in the preceding paragraph of the reaction container 702. If a CVD reaction occurs into a reaction container, the thin film of strontium titanate will be formed in the substrate front face laid in the susceptor 711 held at the heater 710 at constant temperature.
[0086] The above-mentioned CVD process is performed on condition that the following, in order to realize good step coverage and the good perovskite crystal structure.
[0087] Sr2 (DPM) It is the flow rate of 0.005 sccm about a raw material solution, and the raw material solution of TiO (DPM)2 is supplied by the flow rate of 0.025 sccm. The amount of each raw material supplied to a substrate in this condition is Sr (DPM)2. 50 mmol/m2 and TiO2 (DPM) 250 mmol/m2 It becomes. Moreover, the partial pressure within a reaction container is each. 0.1 Torr And it is set to 0.5 Torr. in order to realize good step coverage on the other hand -- the membrane formation rate of Sr and Ti -- a reaction -- it becomes rate-limiting -- as -- membrane formation temperature 450 degrees C and membrane formation pressure CDV of the strontium titanate film is performed on condition that 50 Torr.

[0088] In this way, after forming the strontium titanate film, it is made to crystallize by performing annealing under ordinary pressure in the oxygen ambient atmosphere of 700 **. In this way, the obtained strontium titanate film has good step coverage, and, moreover, has the good perovskite crystal structure. Moreover, when the dielectric constant was evaluated using platinum as a vertical electrode, it is thickness about strontium titanate. At the sample of 50 nm, they are the non-dielectric constant 200 and thickness. At the sample of 25 nm, it is a non-dielectric constant. It was 170. This value is a high value equivalent to the value (K.Abe et al., J.Appl.Phys., 32, and 4186 (1993)) acquired by the conventional spatter.
[0089] As mentioned above, although the manufacture approach of the semiconductor device by this invention was explained using the example, this invention can add various modification, unless it is not limited to these examples and deviates from the essence of this invention. For example, this invention persons are N2 as carrier gas used in the case of chemical vapor deposition. And even if it is the case where helium is used, it is checking that this effect of the invention is attained. Moreover, although the C11H19O2 compound (DPM) is used as a beta diketone complex compound in the above-mentioned example, it is C5 HF 6O2 besides this. If it is beta diketone compounds of Ba, Sr, and Ti, such as a compound (HFA), it will also check that there is no change in effectiveness. Furthermore, it is O2 as an oxidizer. Also when what activated nitrogen oxides (Nx Oy) like N2 O, NO2, and NO, and O3, C4 H4 O, C4 H8 O or these gas with the plasma or light is used instead, it is checking that the same effectiveness is acquired.
[0090] Moreover, it is possible for it not to be limited to an example about any members other than a dielectric thin film, and to perform various deformation. for example, the up electrode and lower electrode of storage capacitance may not be restricted to Pt, and other metals, such as Ir, are sufficient as them -- carrying out -- PtOx and IrOx etc. -- conductive metallic oxide is sufficient and SrTiO3 which added Nb further and gave conductivity, ITO, etc. are sufficient. In the above-mentioned example, although the example which applied the manufacture approach of this invention to DRAM was explained, it is also possible to apply to semiconductor devices other than DRAM, of course.

[Translation done.]

* NOTICES *

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The graph which took the growth rate of a thin film along the axis of ordinate, took the growth temperature of a thin film along the axis of abscissa, and showed the temperature dependence of a growth rate in order to explain vocabulary called "reaction rate-limiting conditions" and "supply rate-limiting conditions" of being used in this specification.
[Drawing 2] SrTiO3 Graph which shows the temperature dependence of Sr rate of sedimentation and Ti rate of sedimentation when supplying Sr raw material and Ti raw material of a constant rate to a CVD chamber about the case where the film is deposited.
[Drawing 3] The graph which shows that the rate of sedimentation of Pb, Ti, and Zr when supplying Pb raw material, Ti raw material, and Zr raw material of a constant rate to a CVD chamber ********** about the case where the PZT film is deposited.
[Drawing 4] Sr2 (DPM) Graph which shows the situation that the decomposition temperature Tc in a gaseous phase changes depending on oxidizer conditions.
[Drawing 5] The explanatory view showing the situation that the smooth nature of the front face of a thin film deteriorates when forming a high dielectric thin film by CVD in reaction rate-limiting conditions.
[Drawing 6] The graph which shows that the dielectric constant of strontium titanate has a presentation dependency.
[Drawing 7] The graph which shows that Sr/(Sr+Ti) ratio of deposition ****** change depending on membrane formation temperature when strontium titanate is formed by CVD, supplying a raw material so that Sr/(Sr+Ti) ratio in material gas may be set to 0.5.
[Drawing 8] Drawing showing the outline of the chemical-vapor-deposition equipment used for formation of a dielectric thin film in the example of this invention.
[Drawing 9] Drawing showing the cross section of Si substrate before forming a thin film in the example of this invention.
[Drawing 10] It is SrTiO3 at reaction rate-limiting conditions on Si substrate which shows a cross section to drawing 9 in the example of this invention. Drawing showing the cross section of Si substrate after forming a thin film.
[Drawing 11] It is SrTiO3 at supply rate-limiting conditions on Si substrate which shows a cross section to drawing 9 in the example of this invention. Drawing showing the cross section of Si substrate after forming a thin film.
[Drawing 12] It is Ti (OC three H7)4 as a Ti raw material on Si substrate which shows a cross section to drawing 9 in the example of this invention for a comparison. It uses and is SrTiO3 at supply rate-limiting conditions. Drawing showing the cross section of Si substrate after forming a thin film.
[Drawing 13] Bax Sr1-x TiO3 produced in the example of this invention Drawing showing the cross section of the dynamic random access memory cell which has trench capacitor structure constituted considering the thin film as a capacitor insulator layer.
[Drawing 14] Bax Sr1-x TiO3 produced in the example of this invention Drawing showing the cross

section of the dynamic random access memory cell which has SUTAKKUTO capacitor structure constituted considering the thin film as a capacitor insulator layer.
[Drawing 15] The sectional view having shown order for the production process of a DRAM cel later on in order to explain other examples of this invention.
[Drawing 16] The sectional view having shown order for the production process of a DRAM cel later on in order to explain other examples of this invention.
[Drawing 17] The sectional view having shown order for the production process of a DRAM cel later on in order to explain another example of this invention.
[Drawing 18] Drawing showing the outline of the chemical-vapor-deposition equipment used for formation of a dielectric thin film in still more nearly another example of this invention.
[Drawing 19] Drawing showing the outline of the chemical-vapor-deposition equipment used for formation of a dielectric thin film in still more nearly another example of this invention.
[Description of Notations]
101 -- A reaction container, 102,601 -- Si substrate, 103 -- Resistance heating heater, 104 -- A thermocouple, 105,161,162 -- A pressure detector, 106,151,152 -- Pressure control valve, 107 -- A vacuum pump, 108 -- A gate valve, 111,112 -- Raw material restoration container, 113 -- An argon gas supply line, 114 -- A material gas supply pipe, 115,118 -- Exhaust pipe, 116 -- An oxygen gas supply pipe, 121, 122, 123,124,125,126 -- Mass flow rate controller, 131,132,133 -- A bulb, 141,142,143 -- Passage change machine, 171,172 [Thin film,] -- Raw material heating oven, 173 -- Piping heating oven 201, 202, and 203,204,205,206 -- SrTiO3 302 [-- The source and a drain 306 / -- An oxide film, 307 / -- Pt lower electrode, 308 / -- Ba0.45Sr0.55TiO3 / The storage capacitance film, 609 -- Pt up electrode] -- An isolation oxide film, 303 -- Gate oxide, 304 -- A polycrystal silicon-gate electrode, 305

[Translation done.]

* NOTICES *

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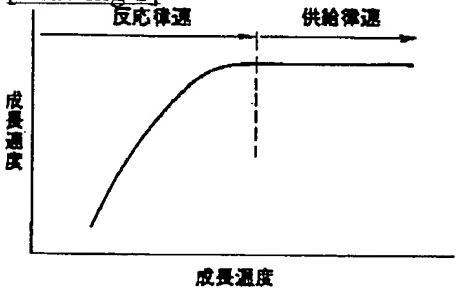
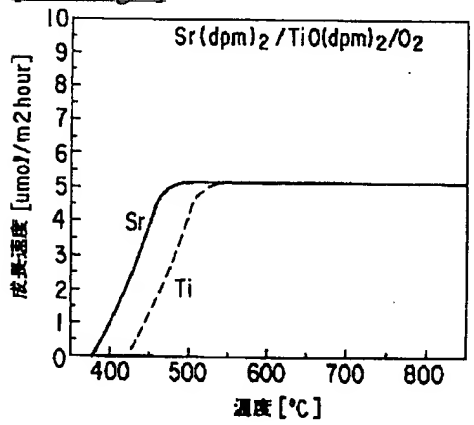
DRAWINGS

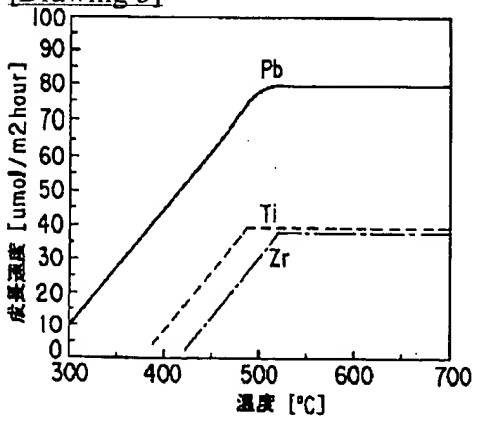
[Drawing 1]



[Drawing 2]



[Drawing 3]



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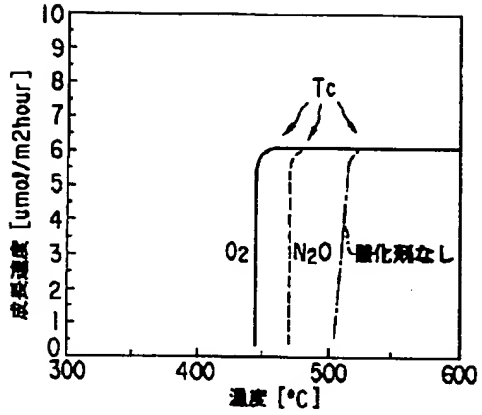

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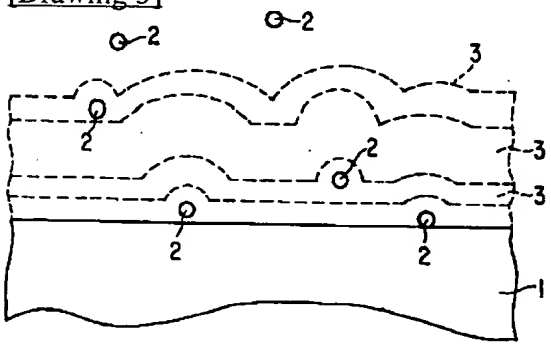
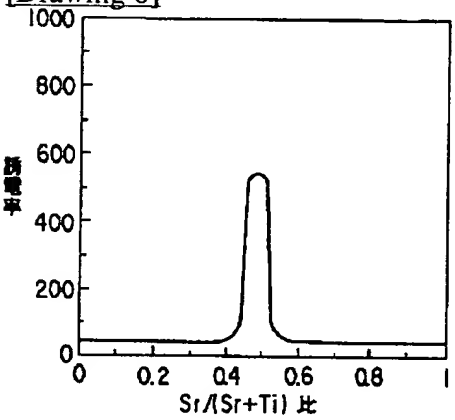
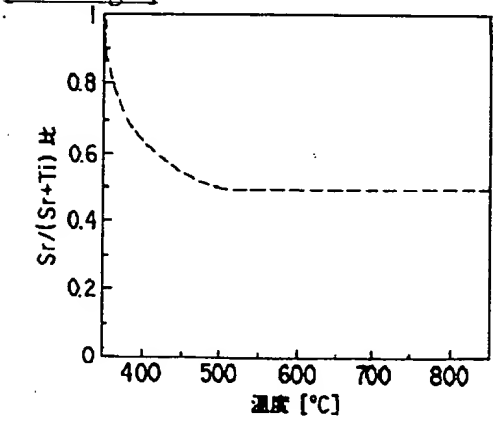


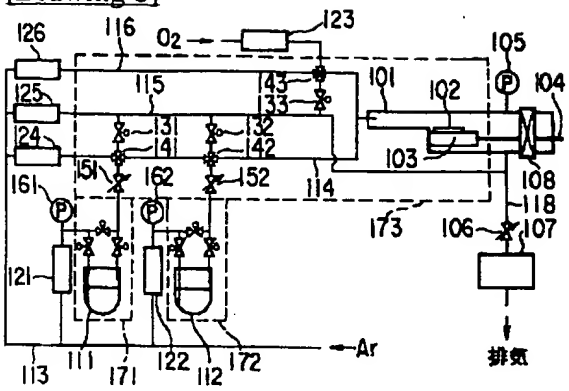
[Drawing 6]



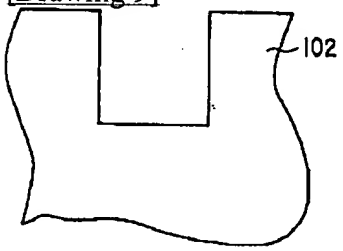
[Drawing 7]



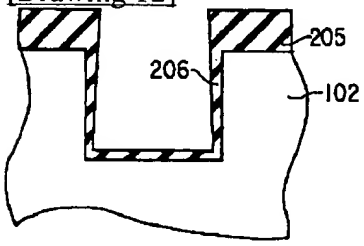
[Drawing 8]



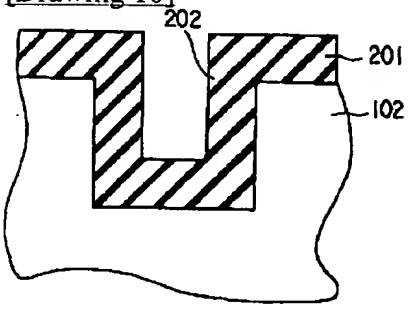
[Drawing 9]



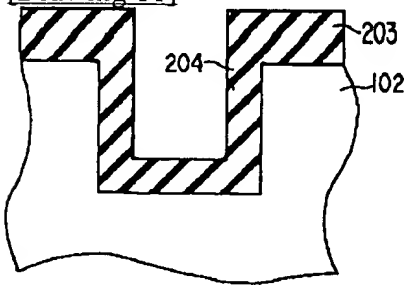
[Drawing 12]



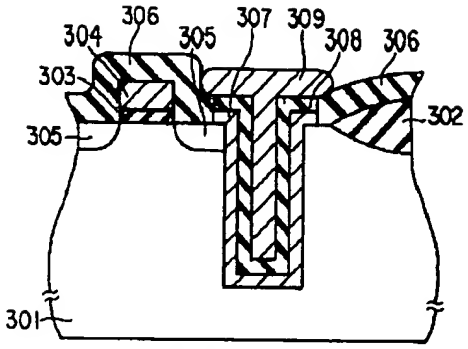
[Drawing 10]



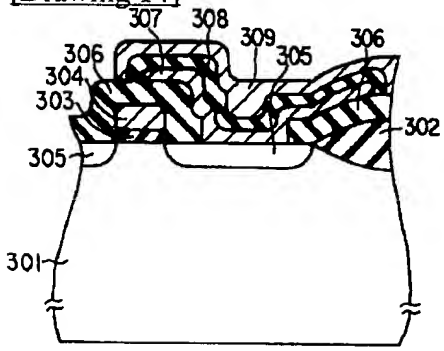
[Drawing 11]



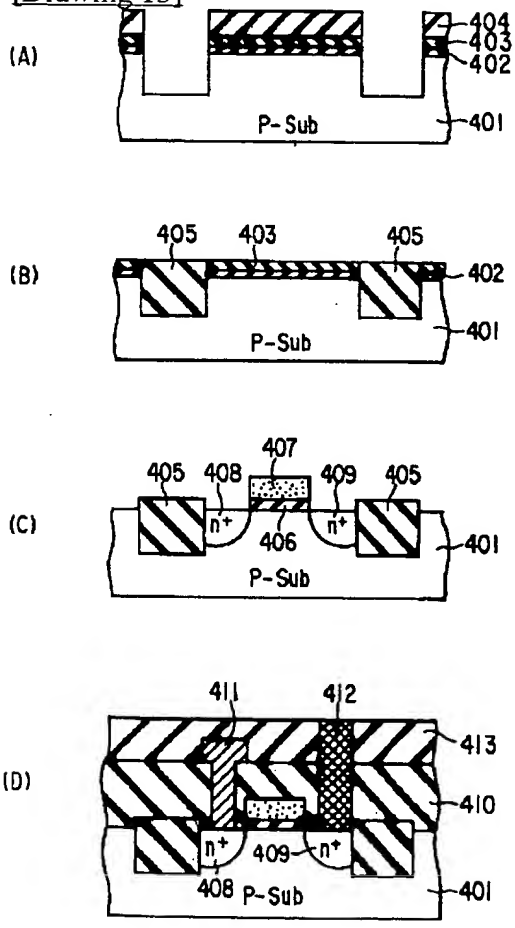
[Drawing 13]



[Drawing 14]



[Drawing 15]



[Drawing 16]

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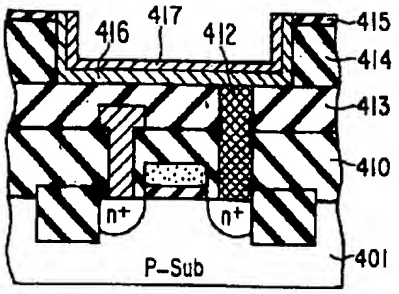

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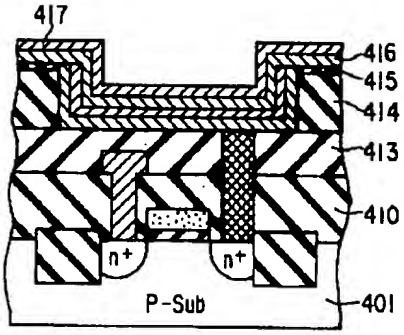

[Drawing 17]

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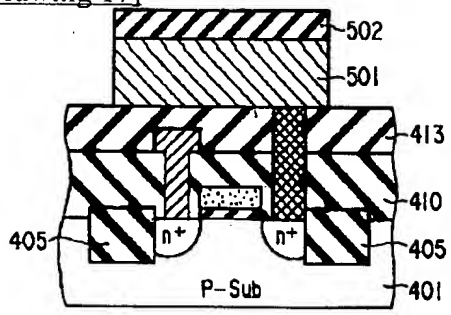

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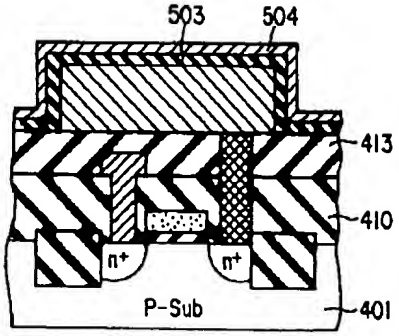
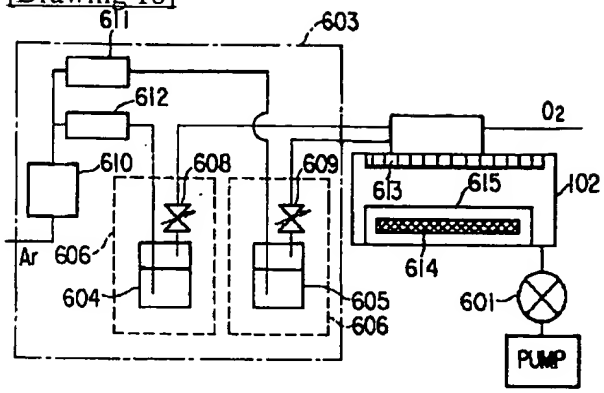
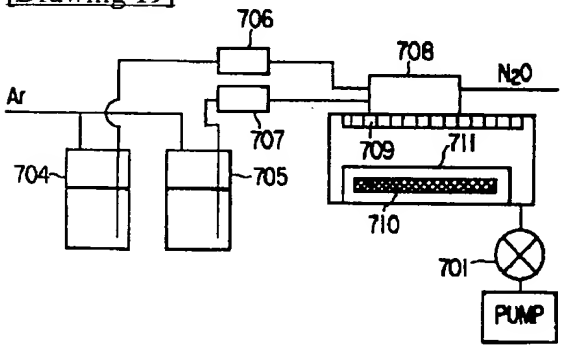


[Drawing 18]



[Drawing 19]



[Translation done.]